(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 663 719 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
03.04.2002 Bulletin 2002/14

(51) Int Cl.[7]: **H03F 3/45**

(21) Application number: **94309627.1**

(22) Date of filing: **21.12.1994**

(54) Analog filter circuit and semiconductor integrated circuit device using the same

Analoge Filterschaltung und integrierte Halbleiterschaltungsanordnung mit dieser Schaltung

Circuit de filtrage analogique et dispositif de circuit intégré à semi-conducteur l'utilisant

(84) Designated Contracting States:
DE FR GB IT

(30) Priority: **12.01.1994 JP 174794**

(43) Date of publication of application:
19.07.1995 Bulletin 1995/29

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EP 0 663 719 B1

Description

[0001] The present invention relates to an analog signal processing technique and, more particularly, to a technique which is especially effective when applied to an analog filter circuit using a differential amplifier whose transconductance is controllable, such as a technique which is effective when applied to a semiconductor integrated circuit device (hereinafter also referred to as an LSI) having an analog filter circuit therein and used in a device such as a portable telephone operating on a low voltage.

[0002] In recent years, as portable telephones and battery-operated electronic devices (e.g., notebook computers and cassette tape recorders) have become popular, a demand of lowering the voltage and reducing the power consumption of an LSI has been rising so as to further reduce the size and weight of the devices and to prolong the service life of the device with small-sized batteries.

[0003] On the other hand, degitalization has come in the communications and audio fields. Since, however, the voices, images and electric waves processed are analog signals, analog circuits are indispensable. In the signal processing for the digital communications, moreover, there are required A-D converters, D-A converters and analog filters which are disposed before and after the converters so as to remove aliasing noises and high-frequency components.

[0004] However, the performance of analog circuits highly depends upon the power supply voltage, and contrivance is required for lowering the voltage. Particularly, the key techniques are A-D and D-A converters and the filter circuit, and current-driven A-D and D-A converters are now under development. Therefore, another major problem left unsolved is to realize a filter circuit which operates on a low voltage with a low power consumption and has little frequency deviation.

[0005] As analog filter circuits a CR filter using a resistor R and a capacitor C and a switched capacitor filter in which the resistor of the CR filter is replaced by a switch. The CR filter is a continuous-time filter, and the cut-off frequency fc (the frequency at a gain of -3 dB) is expressed by $1/2\pi$ RC, so that the cut-off frequency fc varies ± 50% at the maximum due to production variation (± 30%) of the resistor R and the production variation (± 20%) of the capacitor C. We have found out that the CR filter has a problem that frequency deviation is very bad.

[0006] On the other hand, the switched capacitor filter is a discrete-time filter, and the cut-off frequency fc is expressed by $fs \cdot C1/C2$ where fs is a sampling frequency. Since the cut-off frequency fc of the switched capacitor filter is thus determined by the sampling frequency and the capacity ratio of the capacitor used in the filter, the switched capacitor-filter exhibits remarkably excellent characteristics in the frequency deviation. We have found another problem that a high-speed amplifier is required which can follow a frequency ten or more times higher than the signal frequency.

[0007] Moreover, the switched capacitor filter requires a continuous-time front- and back-end filters, so that it is not suitable for reducing the power consumption. The MOSFETs constituting switches are not turned on if the supply voltage is low, so that it is not suited also for lowering the voltage. In this case, there can be considered a method of boosting the clocks for turning on and off the switches. However, the so-called "feed-through", in which the gate voltage is transmitted to the source or drain through a parasitic capacitor between the gate and the source or between the gate and the drain, increases to deteriorate the SN ratio (Signal-to-Noise ratio).

[0008] As an analog filter circuit capable of operating on a low voltage with a power consumption, moreover, there has been proposed an operational transconductance amplifier-capacitor (hereinafter also referred to as an OTA-C) filter, as shown in Fig. 19, in which a differential amplifier circuit (Operational Transconductance Amplifier, hereinafter also referred to as an OTA) whose transconductance Gm (the voltage-current conversion characteristic) is controllable used in place of the resistors of the CR filter. The OTA-C filter has an advantage that the cut-off frequency fc is expressed by $Gm/2\pi C$ and the deviation of the cut-off frequency fc can be compensated by adjusting the transconductance Gm of the differential amplifier in accordance with the amount of variation of the capacitance C. According to our study, however, the distortion of the OTA-C filter cannot be limitted to below 0.2%, so that it does not satisfy the practical requirement.

[0009] Therefore, we have investigated the cause that the operating voltage of the OTA-C filter cannot be lowered. The Gm-controllable amplifier used in the OTA-C filter comprises a differential amplifier, as shown in Fig. 18. Then, it can be considered that the transconductance Gm is adjusted by adjusting the gate voltage Vc of a constant current MOSFET M5 to change a bias current Ic.

[0010] In the basic circuit of Fig. 18, the gate of a MOSFET M1 connected as a load to the drain terminal of an input differential MOSFET M3 is connected to the drain. In short, the MOSFET M1 is, so-called, diode-connected. As a result, in cases where the supply voltage VDD is low, and the voltage Ve (the difference of Vgs-Vth between the gate-source voltage Vgs and the threshold voltage Vth of the MOSFET M3) and the threshold voltages of the P-MOSFETs M1 and M2 are high, the voltage at a node N1, i.e., the drain voltage of the MOSFET M3 drops, causing the MOSFET M3 to be unsaturated when the input signal Vin rises. Our investigations have reached a conclusion that the above process is the cause that a low-voltage OTA-C filter cannot be realized. If the MOSFETs operate in an unsaturated range, distortion will arise in the change in the output signal due to the change in the input signal. If, in the OTA, the MOSFETs also operate in an unsaturated

range, the straightness (linearity) between the input voltage and the output voltage is deteriorated.

[0011] The present invention has been achieved against the background described above and has an object to provide a filter circuit which operates on a low voltage with a low power consumption and has a low distortion and a small frequency deviation.

[0012] DE-U-9300550.4 discloses an analog filter circuit having a voltage/current conversion circuit with inversion and non-inversion input and output nodes, in which the inversion output node is connected to the non-inversion input node, the non-inversion output node is connected to the inversion input node and capacitance circuit is connected to the non-inversion output node. The conversion circuit has two differential MOSFETs whose drains respectively provide output signals to the inversion and non-inversion output nodes. Respective current circuits are connected between the power supply terminal and the drain of the differential MOSFETs and a current source is connected to the source of the first differential MOSFET. Thus DE-U-9300550.4 corresponds to the pre-characterising part of claim 1.

[0013] According to a first aspect of the invention there is provided an analog filter circuit comprising:

(i) a voltage/current conversion circuit having an inversion input node, a non-inversion input node for receiving an input voltage signal, an inversion output node and a non-inversion output node (OUT^+) coupled to the inversion input node;

the inversion output node of the voltage/current conversion circuit being coupled to the non-inversion input node of the voltage/current conversion circuit, the voltage/current conversion circuit having a first differential MOSFET having a source, a drain providing a first output signal to the inversion output node and a gate, a second differential MOSFET having a source, a drain providing a second output signal to the non-inversion output node and a gate, a current source connected to the source of said first differential MOSFET, a first current circuit connected between a power supply terminal to which a predetermined voltage is applied and the drain of said first differential MOSFET;

and a second current circuit connected between said power supply terminal and the drain of said second differential MOSFET;

(ii) a capacitance circuit connected to the non-inversion output node of said voltage/current conversion circuit; and

(iii) a control circuit connected to the first current circuit and the second current circuit of said voltage/current conversion circuit, and used to determine the current values of the first and second current circuits; wherein the gate of the first differential MOSFET receives a first input signal from the non-inversion input node, the gate of the second differential MOSFET receives a second input signal from the inversion input node, and the source of the first differential MOSFET is connected to the source of the second differential MOSFET.

[0014] According to a second aspect of the invention there is provided an analog filter circuit formed on a semiconductor substrate, comprising:

a plurality of voltage/current conversion circuits,
a plurality of capacitance circuits connected to the respective non-inversion output nodes of said plurality of voltage/current conversion circuits; and
a control circuit is provided common to said plurality of voltage/current conversion circuits,

wherein each of said voltage/current conversion circuits includes:

an inversion input node, a non-inversion input node for receiving an input voltage signal, an inversion output node and a non-inversion output node coupled to the inversion input node, the inversion output node of the voltage/current conversion circuit being coupled to the non-inversion input node of the voltage/current conversion circuit, and including:

a first differential MOSFET having a source, a drain providing a first output signal to the inversion output node and a gate;
a second differential MOSFET having a source, a drain providing a second output signal to the non-inversion output node and a gate;
a current source connected to the source of said first differential MOSFET;
a first current circuit connected between a power supply terminal to which a predetermined voltage is applied and the drain of said first differential MOSFET; and
a second current circuit connected between said power supply terminal and the drain of said second differential MOSFET;
whereas a control circuit is provided common to said plurality of voltage/current conversion circuits, said control circuit is connected to the first and second current circuits of each of said voltage/current conversion circuits, used to determine the current values of the first and second current circuits; and
in each said gate of the first differential MOSFET receives a first input signal from the non-inversion input node, the gate of the second differential MOSFET receives a second input signal from the inversion input node, and the source of the first differential MOSFET is connected to the source of the second differential MOSFET.

[0015] The present invention may thus enable a filter

circuit to be produced which is suitable for an LSI having a digital circuit and an analog circuit mixedly.

[0016] The present invention may also enable a differential amplifier to be produced which has a stable transconductance.

[0017] The present invention may also enable a low voltage/low power consumption LSI to be produced. A Gm-controllable amplifier used in an OTA-C filter is so structured that a constant voltage from a bias circuit is applied to the gates of load MOSFETs connected to the drains of input differential MOSFETs of a basic differential amplifier to allow the load MOSFETs to operate as constant current sources and by connecting the inverted output terminals of the circuit to the input terminals of the differential amplifier.

[0018] More preferably, the differential amplifier is equipped with a current compensation type bias generator for generating a bias voltage corresponding to the level of the input voltage monitored, and applying the bias voltage to the gates of constant current MOSFETs of the differential amplifier, so as to compensate the current fluctuation due to the channel length modulation effect.

[0019] By the aforementioned means, the MOSFETs acting as the loads of the input differential MOSFETs are made to constant current sources, so that the drain voltages of the input differential MOSFETs become independent of the threshold voltage of the constant current type load MOSFETs. Even if the supply voltage is set to as low as about 1.5 V, the input differential MOSFETs can be prevented from being unsaturated when input signals rise. If, moreover, the differential amplifier has a single-ended output structure where the output voltage only from the non-inverted output terminals, the current outputted from the inverted output terminals and flowing in the opposite direction to the non-inverted output terminals is absorbed by changing the drain voltage of the input differential MOSFETs, and accordingly the circuit balance cannot be maintained. If, however, the inverted output terminals are connected to the input terminals, the currents outputted from the inverted output terminals and flowing in the opposite direction to the non-inverted output terminals can be absorbed from the non-inverting input terminals, so that the balance of the circuit can be easily maintained. Moreover, since the drain voltage of the input differential MOSFETs similarly fluctuates, the symmetry can be improved to reduce the distortion.

[0020] Since, furthermore, the current fluctuation due to the channel length modulation effect that the pinch-off point of a MOSFET approaches the source to increase the drain current when the drain-source voltage rises, can be compensated, the bias current of the differential amplifier is constant, stabilizing the transconductance and reducing the output distortion.

[0021] In the drawings:

Fig. 1 is a circuit diagram showing one embodiment of a Gm-controllable differential amplifier according to the present invention;

Fig. 2 is a circuit structural diagram showing an example of a primary low-pass filter using the differential amplifier of Fig. 1;

Fig. 3 is a graph showing the dependency of the distortion on a channel in the differential amplifier of Fig. 1;

Fig. 4 is a circuit diagram showing a second embodiment of a Gm controllable differential amplifier according to the present invention;

Fig. 5 is a circuit diagram showing a third embodiment of a Gm controllable differential amplifier according to the present invention;

Fig. 6 is a circuit diagram for explaining the operation of a bias circuit of the differential amplifier of Fig. 4;

Fig. 7 is a circuit diagram showing a fourth embodiment of a Gm controllable differential amplifier according to the present invention;

Fig. 8 is a circuit diagram showing an example of a bias circuit suitable for the differential amplifier of Fig. 7;

Fig. 9 is a block diagram showing one embodiment of a primary low-pass filter using a Gm-controllable differential amplifier according to the present invention;

Fig. 10 is a circuit diagram showing one embodiment of a control voltage generator (a slave filter and a phase difference detecting/adjusting circuit) of the embodiment of Fig. 9;

Fig. 11(a) to Fig. 11(d) are waveform explanatory diagrams showing the input/output waveforms of the phase difference detecting/adjusting circuit of the embodiment of Fig. 10 in relation to frequency;

Fig. 12 is a block diagram showing one embodiment of a ternary low-pass filter using a Gm-controllable differential amplifier according to the present invention;

Fig. 13 is a block diagram showing another embodiment of a ternary low-pass filter using a Gm controllable differential amplifier according to the present invention;

Fig. 14 is a block diagram showing one example of a ternary CR low-pass filter of the prior art;

Fig. 15 is a block diagram showing a circuit example in cases where the resistors in the CR low-pass filter of Fig. 14 are simply replaced by the Gm-controllable differential amplifier according to the present invention;

Fig. 16 is a block diagram showing an example of the construction of a radio communication system as an application example of the filter circuit according to the present invention;

Fig. 17 is an explanatory diagram showing the relation between the cut-off frequency and the phase delay of the primary low-pass filter;

Fig. 18 is a circuit diagram showing one example of a devisable Gm-controllable differential amplifier;

and

Fig. 19 is a circuit structural diagram showing one example of the primary low-pass filter using the differential amplifier of Fig. 18.

[0022] Figs. 1 and 2 show one embodiment of a Gm controllable differential amplifier according to the present invention and an OTA-C filter using the amplifier. Here in the Figures, MOSFETs (e.g., M3, M4 and M5) having arrows directed outward from their gate terminals is of an N-channel type, whereas MOSFETs (e.g., M1 and M2) having arrows directed to their gate terminals is of a P-channel type.

[0023] The differential amplifier of the embodiment includes a differential amplifier stage OTA and a bias circuit BIAS. The differential amplifier stage OTA comprises input differential MOSFETs M3 and M4, load MOSFETs M1 and M2 made to serve as constant current sources and connected to the drains of the input operational MOSFETs M3 and M4 and constant current MOSFET M5. The gate bias voltage of the load MOSFETs M1 and M2 is generated by the bias circuit BIAS. Moreover, this bias circuit BIAS is provided for generating the gate bias voltage of the MOSFETs M1 and M2. This bias circuit BIAS also generates the gate bias voltage of the constant current MOSFET M5 which is connected to the common source of the input operational MOSFETs M1 and M2. In other words, the connections are so made that the source-drain path of the input differential MOSFET M3 (M4) is connected in series to the source-drain path of the load MOSFET M1 (M2) and further in series to the source-drain path of the constant current MOSFET M5.

[0024] In the differential amplifier of the embodiment, the amplitude of an input signal Vin for the MOSFETs M1 to M5 to operate in the saturated region is not dependent upon the threshold voltage Vthp of a P-channel type load MOSFET, because it melts the following conditions, so that the voltage can be lowered:

$$2Ve + Vthn < Vin < VDD - Ve.$$

Here, the voltage Ve is a difference (Vgs - Vthn) between a gate-source voltage Vgs of the MOSFETs M3 and M4 and the threshold voltage Vthn of the same MOSFETs, and the amplitude of the input signal Vin takes a value of 0.31 V if the voltage Vthn is 0.25 V.

[0025] In the differential amplifier of the embodiment, on the other hand, a current Iout flowing from the output terminal out+ is a half of that of the circuit of the prior art. Hence, the transconductance Gm is expressed by the following Equation:

$$Gm = Iout/\Delta Vin = \sqrt{(Ic \cdot \beta \cdot W/L)}/2.$$

Here, β, W and L designates the values which are determined by the MOSFETs M3 and M4. The value β is the channel conductance of the MOSFET; L is a channel length along the channel; and W is the channel width in the direction orthogonal to the channel.

[0026] In the differential amplifier of the embodiment, however, a problem rises in the current Iout- which is outputted from an inverted output terminal out- and flows in the direction reverse to that of the aforementioned current Iout. If there is no part to which the current Iout- is fed, it tends to be absorbed by the change of the drain voltage of the MOSFET M3, so that the voltage of the inverted output terminal out- greatly fluctuates and the balance of the circuit cannot be kept. In this case, there is used a differential output method in which a capacitor is connected between the inverted output terminal out- and a non-inverted output terminal out+. In the filter circuit of the present application, it is desirable that the differential amplifier has a single-ended output. In the differential amplifier of the embodiment, therefore, a non-inverting input terminal (in+) and the inverted output terminal (out-) are connected so that the current (Iout) flowing in the direction opposite to that of the non-inverted current outputted from the non-inverted output terminal (out-) may be absorbed from the non-inverting input terminal (in+).

[0027] Here will be described the bias circuit BIAS.

[0028] The bias circuit BIAS in the differential amplifier comprises: MOSFETs MB0 and MB1 connected in series between the supply voltage VDD and the ground potential, and MOSFETs MB2 and MB4 also connected in series between the supply voltage VDD and the ground potential. The MOSFET MB1 on the ground potential side constitutes a current mirror circuit in which the gate and drain are connected to apply the drain voltage to the gates of the MOSFETs MB1, MB2 and MOSFET M5 current supply of the differential amplifier stage OTA.

[0029] Moreover, the MOSFET MB2 of the bias circuit BIAS is structured as a diode-connection circuit, in which the gate and drain are connected to apply the drain voltage to the gate terminals of the aforementioned constant current type load MOSFETs M1 and M2 of the differential amplifier stage OTA. The Gm of the differential amplifier state OTA is controlled by applying a Gm controlling control voltage Vc to the gate of the MOSFET MB0 of the bias circuit BIAS and by feeding a bias current according to the level of the voltage Vc to the constant current MOSFETs M1, M2 and M5.

[0030] Specifically, as the level of the Gm controlling control voltage Vc rises, the current of the MOSFET MB0 is reduced to lower the gate voltage of the current-mirror connected MOSFETs MB1, MB4 and MB5, and thereby to reduce the bias current of the differential amplifier stage. As the level of the Gm controlling control voltage Vc drops, on the other hand, the current of the MOSFET MB0 increases to raise the gate voltage of the current-mirror connected MOSFETs MB1, MB4 and MB5, and thereby to increase the bias current of the dif-

ferential amplifier stage.

[0031] Moreover, the embodiment is so constructed that even if the supply voltage VDD is set to a voltage as low as 1.5 V, the bias voltage to prevent the input differential MOSFETs M3 and M4 from becoming unsaturated in response to the input signal Vin of 0.91 V to 1.22 V is produced by the aforementioned bias circuit BIAS and is applied to the gates of the constant current type load MOSFETs M1 and M2.

[0032] As a result, in a circuit simulation using a 0.8 μm analog-digital process model parameter the distortion caused by the circuit system of the embodiment was able to be reduced to 0.12% in the primary filter (cut-off frequency fc = 30 KHz) when the supply voltage was 1.5 V, the input signal was 1.05 ± 0.15 V and the input frequency was 10.5 KHz.

[0033] Incidentally, in the differential amplifier of the embodiment, the distortion is 0.02% if the MOSFETs M1, M2 and M5 are assumed to be an ideal current source. It is therefore deduced that the distortion (0.12%) of the aforementioned simulation is resulted from the fact that the drain voltages of the MOSFETs M1, M2 and M5 fluctuate according to the changes in the input/output signals, and the current is changed by the channel length modulation effect.

[0034] In this embodiment, therefore, the fluctuations of the drain voltages due to the channel length modulation effect are suppressed to reduce the output distortion of the differential amplifier by setting the channel lengths of the aforementioned MOSFETs M1, M2 and M5 to about 6 μm.

[0035] Fig. 3 shows the relation between the distortion of the differential amplifier and the channel length of the MOSFET M5. Here, Fig. 3 shows the result of measurement which is obtained setting the ratio W/L of the channel width to the length to a constant so that a current of identical magnitude may flow through the MOSFET M5.

[0036] It is known in the prior art that the channel length modulation effect of a MOSFET can be lowered by increasing the channel length. However, our investigations have revealed that in a differential amplifier the output distortion is minimized for the channel length of about 6 μm of the MOSFET M5 but degraded for the larger channel length. This is because although an increase in the channel length will reduce the amplitude of the current error due to the channel length modulation effect, the parasitic capacitance Cs (the drain capacitance of M5) applied to a node N2 of the circuit of Fig. 1 increases to augment the current error due to the current flowing through the parasitic capacitor Cs. From the above description, it is understood that it is advantageous that for the differential amplifier of Fig. 1 N-channel type MOSFETs M3, M4 and M5 having large β (channel conductance) values be used.

[0037] Figs. 4 and 5 show second and third embodiments a Gm-controllable differential amplifier according to the present invention and an OTA-C filter using the amplifier. In Fig. 4 showing the second embodiment, the elements designated by the same labels as those of Fig. 1, are the identical elements.

[0038] The distortion of the differential amplifier of this embodiment is further reduced by improving the circuit of the embodiment of Fig. 1 so that the current of the constant current MOSFET M5 may be compensated according to the change in the input signal. In the circuit of Fig. 1, as the input voltage lowers, the potential of the node N2 accordingly lowers to decrease the current of the MOSFET M5. As the input voltage rises, the potential of the node N2 accordingly rises to increase the current of the MOSFET M5. In the circuit of Fig. 4, therefore, the bias circuit BIAS is so improved that the gate voltage of the MOSFET M5 is raised or lowered to compensate the current increase or decrease of the aforementioned MOSFET M5 so that the current may be held at a constant value.

[0039] Specifically, to the constant current MOSFET M5 of the differential amplifier OTA, there is connected in a current mirror manner a MOSFET MB11 which is disposed in the bias circuit BIAS. To the MOSFET MB1 fed with a current according to the control voltage Vc, and also to the MOSFET MB4, there is connected in a current-mirror manner MOSFETs MB5, MB6 and MB7 which are connected in series between the supply voltage VDD and the ground potential.

[0040] Between the MOSFETs MB2 and MB4 connected in series between the supply voltage VDD and the ground potential, there is connected a MOSFET MB3 adapted to receive the input signal at its gate terminal. To the MOSFET MB2, moreover, there is connected in a current mirror manner a MOSFET MB8 whose source terminal is connected to the supply voltage VDD. Between the drain terminal of the MOSFET MB8 and the ground potential, there is connected a MOSFET MB9 which is connected in a current mirror manner to the aforementioned MOSFET MB6. To the drain terminal of the MOSFET MB8, there is connected the gate terminal of a MOSFET MB10 which is connected in series to the MOSFET MB11.

[0041] In Fig. 5 showing the third embodiment, the elements designated by the same labels as those of Fig. 4, are the identical elements.

[0042] Next, will be described the portions different from those of the circuit of Fig. 4.

[0043] In the third embodiment, furthermore, unlike the second embodiment, the aforementioned MOSFET MB5 is connected in a current mirror manner to MOSFETs MB12 and MB15. Between the drain terminal of the MOSFET MB12 of the two and the ground potential, there are connected in series a MOSFET MB13 whose gate terminal receives the source voltage of the MOSFET MB3, and a diode-connected MOSFET MB14. Between the drain terminal of the MOSFET MB15 and the ground potential, there are connected in series diode-connected MOSFETs MB16 and MB17 which form a series of MOSFETs in contrast to the series of the MOSFETs MB5, MB6 and MB7.

[0044] To the MOSFET MB16, furthermore, there is connected in a current mirror manner the MOSFET MB18, of the MOSFETs MB18 and MB19 which are connected in series between the supply voltage VDD and the ground potential. The MOSFET MB19 is connected in a current mirror manner to the MOSFET MB14. To the connecting nodes of these MOSFETs MB18 and MB19, there is connected the gate terminal of a MOSFET MB20. Between the drain terminal of the MOSFET MB20 and the supply voltage VDD, there is connected a diode-connected MOSFET MB21, to which is connected in to current mirror manner the constant current type load MOSFETs M1 and M2 of the differential amplifier.

[0045] With reference to Fig. 6, here will be described the current compensating operation on the side of the constant current MOSFET M5 by the bias circuit.

[0046] In this embodiment, the bias circuit is equipped with a monitor terminal MT for an input signal Bin, to which is connected the gate terminal of the MOSFET MB3 through which a constant current is made to flow by the constant current MOSFET MB4. As a result, the MOSFET MB3 acts as a pseudo input MOSFET, and the source voltage changes with the change of the input signal Bin like the potential of the node N2 of the differential amplifier (like the drain voltage of the constant current MOSFET M5). For example, when the input signal Bin rises, the source voltage of the MOSFET MB3 rises to increase the current flowing through the MOSFET MB2 connected to the drain side. Hence, the current of the MOSFET MB8 connected in a current mirror manner to the MOSFET MB2 is increased to increase the current flowing through the MOSFET MB9.

[0047] On the other hand, since a constant voltage is always applied to the MOSFET MB9 by the MOSFET MB6, the gate-source voltage Vgs rises to raise the gate voltage of the MOSFET MBIO when the current of the MOSFET MB8 increases. As a result, the currents flowing through the MOSFET MB10 and the MOSFET MB11 connected to the gate side of the MOSFET MB10 decrease, and the current flowing through the MOSFET M5 connected in a current mirror manner to the MOSFET MB11 also decreases, so that the current flowing through the MOSFET M5, which tends to increase with the rise of the potential of the node N2 by the channel length modulation effect, can be compensated. When the input signal Bin drops, on the contrary, the bias circuit operates to increase the current through the MOSFET M5, which tends to decrease by the effect of the potential at the node N2.

[0048] The current compensation of the constant current type load MOSFETs M1 and M2 of the embodiment of Fig. 5 are substantially similar to the aforementioned ones except that the potential relation is reverse. The MOSFETs MB12 and MB15 correspond to the MOSFETs MB4 and MB7; the MOSFETs MB14 nd MB19 correspond to the MOSFETs MB2 and MB8; MOSFETs MB18, MB20 and MB21 correspond to the MOSFETs MB9, MB10 and MB11; and MOSFET MB13 corresponds to the MOSFET MB3, respectively. A potential, which is lower by the voltage Vth of the MOSFET MB3 than the input signal Bin, is applied as a monitor input to the gate terminal of the MOSFET MB13 to widen the operating range of the MOSFET MB13.

[0049] Consequently, in the bias circuit of Fig. 5, for example, the gate voltage of the MOSFET MB13 rises, as the input signal Bin rises, reducing the current flowing through the MOSFET MB14 connected to the drain side of the MOSFET MB13. As a result, the current flowing through the MOSFET MB19 connected in a current mirror manner to the MOSFET MB14 decreases to reduce the current flowing through the MOSFET MB18.

[0050] With a decrease in the current flowing through the MOSFET MB19, the gate-source voltage Vgs of the MOSFET MB18 drops, but the gate voltage of the MOSFET MB20 rises. Thereby, the currents flowing through the MOSFET MB20 and the MOSFET MB21 connected to the drain side of the former are increased to augment the currents flowing through the MOSFETs M1 and M2 connected in a current mirror manner to the MOSFET MB21, and thus the currents flowing through the MOSFETs M1 and M2, which tends to decrease by the channel length modulation effect due to the rises of the output voltages out- and out+, can be compensated. When the input signal Bin drops, on the contrary, the bias circuit operates to decrease the current flowing through the MOSFETs M1 and M2, which tends to increase with the drops of the output voltages out- and out+.

[0051] In the bias circuit, as has been described above, the drain voltage of the MOSFET MB4 is fluctuated as at the drain of the constant current MOSFET M5, and the current fluctuation is transmitted from the MOSFET MB2 to the MOSFET MB8 by making use of the current mirror circuit. At the same time, the MOSFET MB9 is biased by a constant voltage. As a result, the potential at the source of the MOSFET MB9, i.e., at the gate of the MOSFET MB10 is reversely fluctuated by the current fluctuation due to the drain fluctuation of the MOSFET MB4 and is fed through the MOSFET MB11 to the gate of the constant current MOSFET M5.

[0052] As a result, the current fluctuation of the constant current MOSFET M5 by the bias circuit is reduced to 0.2%. The distortion in the primary filter, to which is applied the differential amplifier of Fig. 5 of which the currents of the constant current type load MOSFETs M1 and M2 can be also improved to 0.024%.

[0053] Fig. 7 shows another embodiment of the Gm controllable differential amplifier which is suited for use in the OTA-C filter. The differential amplifier of Fig. 7 is improved that a differential amplifier having an excellent Gm linearity, as called cross-couple type, is suited for an OTA-C filter.

[0054] A cross-couple type differential amplifier is such that the drains of two pairs of MOSFETs Q1, Q2, and Q3, Q4 whose sources are commonly connected are commonly cross-connected to each other, constant current source IO are connected to the common drains

respecively, ahd signals whose dc levels are different by VB are fed to the gates of the MOSFETs Q1, Q3, and Q2, Q4. Thus, the differential amplifier of this type is characterized in that the transconductance Gm is not dependent upon the current IC0. As a result, if the W/L (the ratio of the gate width to the gate length) of the MOSFETs constituting the constant current sources IC0 connected to the common sources is designed in advance to a large value, no distortion can be generated even when the output current Iout increases by a high-frequency input.

[0055] In the cross-couple type differential amplifier, however, the gate voltages of the MOSFETs Q1, Q2, Q3 and Q4 fluctuate with the fluctuation of the threshold voltage of the VB generating MOSFETs, and thereby the input amplitude at which all the MOSFETs saturatedly operate decrease. So the cross-couple type differential amplifier is not suitable for a low-voltage filter.

[0056] In the cross-couple type differential amplifier of the embodiment of Fig. 7, at the preceding stages of the differential MOSFETs Q1, Q2, Q3 and Q4, there are provided level shifting MOSFETs Q5, Q6, Q7 and Q8 which are diode-connected. The input signals are shifted up by the source-follower type input MOSFETs Q11 and Q12, then shifted down by the MOSFETs of the same characteristics, and inputted to the differential MOSFETs Q1, Q2, Q3 and Q4.

[0057] Namely, the source voltage of the MOSFET Q11 (Q12) to the gate of which an input signal Bin+ (or Bin-) is fed is inputted to the source terminals of the diode connected MOSFETs Q5 and Q6 (Q7 and Q8), the outputs of which are extracted from their gate terminals and inputted to the gate electrodes of the differential MOSFETs Q1 and Q2 (Q3 and Q4). In the circuit of this embodiment, the difference between the lowered levels of the MOSFETs Q5 and Q6 and the difference between the lowered levels of the MOSFETs Q7 and Q8 are both set to the aforementioned voltage VB.

[0058] Constant current sources are respectively connected to the input MOSFETs Q11 and Q12 and the diode-connected MOSFETs Q5, Q6, Q7 and Q8, of which the MOSFETs Q5 and Q7, and Q11 and Q12 are connected to a constant current source I1 for supplying an equal current whereas the MOSFETs Q6 and Q8 are connected to a variable constant current source IC. In the differential amplifier of this embodiment, therefore, the input potential difference VB can be controlled to change the transconductance Gm by adjusting the current of the variable constant current source IC.

[0059] In this embodiment, on the other hand, the MOSFETs Q5 and Q6 (or Q7 and Q8) are of the source input type and have low impedances. Hence, the currents mutually flow between the MOSFETs Q11 (Q12), and Q5, Q6 (Q7, Q8) so that an expected current will not necessarily flow. In the embodiment, therefore, the currents flowing through the individual MOSFETs can be ensured by providing constant current sources to respective source and drain terminals of the MOSFETs Q11 (Q12), and Q5, Q6 (Q7, Q8).

[0060] In the embodiment of Fig. 7, the distortion can be further reduced by using the current compensation type bias circuit shown in Fig. 4 as the bias circuit for the variable constant current source IC or the constant current sources I0, I1 and IC0. In the embodiment, moreover, the differential MOSFETs Q1, Q2, Q3 and Q4 are of the N-channel type, and the input MOSFETs Q11 and Q12 and the level shirting MOSFETs Q5, Q6, Q7 and Q8 are of the P-channel type. However, they can be constituted of MOSFETs of opposite conductivity type.

[0061] The aforementioned constant current sources I1 and I0 and the variable constant current source IC can be each constructed of a single MOSFET.

[0062] Fig. 8 shows an example of the bias circuit for generating the respective gate bias voltages of the current sources I1, I0 and variable constant current sources IC, in cases where they each comprise one MOSFET.

[0063] Moreover, the constant current sources connected to the sources of the MOSFETs Q5, Q11 (Q7, Q12) may be made common to each other. Likewise, the constant current sources connected to the drains of the MOSFETs Q5, Q11 (Q7, Q12) may be made common to each other.

[0064] In Fig. 8, labels BIAS2 designates a bias circuit for generating bias voltages Vc1 and Vc1' for the current sources I1 and I0, and BIAS1 designates a bias circuit for generating bias voltages Vc2 and Vc2' for the variable constant current source IC. These bias circuits have the same structure as that of the bias circuit BIAS in the embodiment of Fig. 5, and the variation of the current due to the channel length modulation effect can be compensated. In Fig. 8, the elements having the same functions as those of the elements composing the bias circuit BIAS of the embodiment of Fig. 5 are designated by the same labels, and their detailed description will be omitted.

[0065] Incidentally, the control of the transconductance Gm is accomplished by adjusting the voltage applied to the control terminal of the bias circuit BIAS1. The constant voltage Vg is applied to the control terminal of the bias circuit BIAS2 so that the bias circuit BIAS2 performs only the compensation of the current variation due to the channel length modulation effect.

[0066] Here will be described an embodiment in which the control voltage Vc for automatically adjusting the transconductance Gm of the amplifier varying with temperature variation and production variation to a desired value can be automatically produced.

[0067] As shown in Fig. 9, this embodiment includes an OTA-C filter (referred to as master filter) 10 used primarily in a signal processing system, a monitoring filter (hereinafter referred to a slave filter) 20 for monitoring a reference signal Vi having a desired frequency, and a phase difference detecting/adjusting circuit 30 for detecting the phase difference between the output Vo of the slave filter 20 and the reference signal Vi to generate

a feedback signal. This adjusting circuit 30 generates a feedback signal for adjusting the cut-off frequency fc of the slave filter 20 to a desired value by performing a feedback so that the phase difference may become a desired value (45 degrees). The feedback signal is fed as the Gm-controlling control voltage Vc of the master filter 10 to the master filter 10.

[0068] In this embodiment, the slave filter 20 comprises an OTA having the same structure as that of the OTA (a Gm-controllable amplifier) constituting the master filter 10. Thanks to a feature of a semiconductor integrated circuit that the production variations of the transconductance Gm, the temperature characteristics and the capacitance are substantially identical in one semiconductor chip, the cut-off frequency fc of the master filter 10 can be equalized to a desired frequency, i.e., the cut-off frequency fc of the slave filter 20.

[0069] Fig. 10 shows a specific circuit example of the control voltage generator comprising the slave filter 20 and the phase difference detecting/adjusting circuit 30.

[0070] The control voltage generator of this embodiments makes use of the fact that the phase delay of the primary low-pass filter is 45 degrees at the cut-off frequency fc defined by the frequency when the gain is -3 dB (see Fig. 17). That is, the control voltage generator generates the feedback signal (Vc) so that the phase difference becomes 45 degrees by inputting the reference signal having a desired frequency to the slave filter 20 comprising an OTA 21 and a capacitor 22 and by detecting the phase difference between the output Vo of the slave filter 20 and the reference signal Vi by the phase difference detecting/adjusting circuit 30.

[0071] In this embodiment, therefore, the phase difference detecting/adjusting circuit 30 comprises comparators 31 nd 32 for converting the output Vo of the slave filter 20 and the reference signal Vi to rectangular waves (pulses), an exclusive OR gate 33 for receiving those output pulses to produce pulses Vd having a duty ratio corresponding to the phase difference of the output pulses, and an integrator (an OTA 34 and a capacitor 35) for integrating the difference between the output pulses Vd and an ideal pulse signal Vr having a duty ratio of 25%.

[0072] In the control voltage generator of this embodiment, if the cut-off frequency fc of the slave filter 20 is equal to the frequency fi (i.e., fc = fi) of the reference signal Vi, the phase of the output Vo of the slave filter 20 will be delayed by 45 degrees, as has been described before. Thus, the output Vd of the EOR gate 33 has a waveform having a frequency which is twice the frequency of the input reference signal Vi and a duty ratio which is 25 %, or 1/4 of that of the input reference signal Vi, as shown in Fig. 11(a).

[0073] When, on the other hand, the OTA 21 constituting the slave filter 20 does not have a desired Gm value, the cut-off frequency fc fails to coincide with the frequency fi of the reference signal Vi so that the duty ratio of the output pulse Vd of the EOR gate 33 becomes different from 25%. Since the difference between the pulse Vd and the ideal pulse signal Vr having the duty ratio of 25% is integrated by the integrator, the phase delay is small, as shown in Fig. 11(b), if fc>fi, so that the duty of the pulse Vd is reduced to increase the integrated value, i.e., the output voltage (control voltage).

[0074] If fc < fi, on the other hand, the phase delay is so large, as shown in Fig. 11(c), that the duty of the pulses Vd is raised to decrease the integrated value, i.e., the output voltage. The transconductance Gm of the OTA 21 constituting the slave filter 20 is adjusted by this output voltage (the control voltage Vc). Negative feedback is so applied that the cut-off frequency fc of the slave filter 20 is raised when the control voltage Vc drops, but lowered when the control voltage Vc rises. As a result, in a steady state, an automatic adjustment is made to maintain fc = fi. Since this control voltage Vc is also fed to the master filter 10, the cut-off frequency fc of the master filter 10 is also controlled to the frequency fi of the reference signal Vi. Moreover, the cut-off frequency after the automatic adjustment can be arbitrarily set by changing the duty ratio of the ideal pulse signal Vr.

[0075] In the control voltage generator of this embodiment, in order to stabilize the output voltage Vc, it is necessary to make the time constant of the integrator larger than that of the slave filter 20. However, the quicker convergence to the steady state can be achieved for the smaller time constant of the integrator. In this embodiment, therefore, the transconductance Gm of the OTA 34 can be increased during the transition to lower the constant of the integrator but is decreased after the transition to raise the constant of the integrator by controlling the control voltage Vc2 of the OTA 34 constituting the integrator.

[0076] Incidentally, in cases where a plurality of signal processing systems, i.e., two or more master filters are provided on a single semiconductor chip, a control voltage generator of the embodiment can be provided commonly for the two master filters thereby to feed the control voltage Vc from one control voltage generator to each of the master filters.

[0077] Since only a single integrator is provided in the loop, the control voltage generator of this embodiment has an advantage that the system operation is stabilized. The generator has also another advantage that the integrated value is constant, as shown in Fig. 11(d), not influencing upon the accuracy even if the OTAs 21 and 34 and the comparators 31 and 32 are offset.

[0078] Fig. 12 shows another embodiment of the OTA-C filter according to the present invention. The OTA-C filter shown in Fig. 12 is formed on a single semiconductor substrate.

[0079] The filter circuit of Fig. 12 is an application of the present invention to a ternary Butterworth low-pass filter. In Fig. 12, each of the OTA1, OTA2 and OTA3 is a Gm-controllable differential amplifier having the same circuit structure as that of the differential amplifying stage OTA shown in Fig. 5. In each OTA, a bias voltage

VGN for the constant current MOSFET M5 and a bias voltage VGP for the MOSFETs M1 and M2 are fed from the common current compensation type bias circuit BIAS. The inverted output terminals of the differential amplifying stage OTA1 and OTA2 are connected to the input terminal Vin having a low impedance, and the inverted output terminal of the differential amplifying stage OTA3 is connected to the input terminal of the OTA3 having a low impedance.

[0080] Incidentally, the filter circuit of Fig. 12 is a further improvement over the OTA-C filter in which resistors R1, R2 and R3 in the Sallen-Key type low-pass filter shown in Fig. 14 are replaced by OTAs (a Gm-controllable differential amplifiers).

[0081] In other words, the circuit, as shown in Fig. 15 is obtained, when the resistors R1, R2 and R3 in the Sallen-Key type filter shown in Fig. 14 are merely replaced by OTAs. Here, the reason why the resistor R2 is replaced by two OTAs is that an amplifier OTA2 for charging/discharging a capacitor C_1 and an amplifier OTA4 for charging/discharging a capacitor C_2 are required because there are two cases where through the resistor R2, a current I_1 for charging the capacitor C_1 and a current I_2 for charging the capacitor C_2 flow. It has been found out that an identical transmission function can be achieved even if the amplifier OTA of Fig. 15 is omitted, by selecting proper ratios of capacitances C_1, C_2, and C_3 ($C_1 = C_2 = C_3$ in the case of the ternary Butterworth) of the circuit of Fig. 14. Therefore, we have deviced an improved OTA-C filter, as the embodiment in Fig. 12.

[0082] The OTA-C filter, as has been examined, uses a completely differential type amplifier. Since, in this case, a high voltage is applied between the inverting input terminal and the non-inverting input terminal, the linearity of the voltage/current conversion characteristics of the OTA, as it is, represents the linearity of the filter so that the OTA is required to have an extremely high linearity. In the OTA-C filter of the embodiment, on the contrary, a single-ended output amplifier is used, and so the OTA-C filter has an advantage that such an extremely high linearly is not required of the OTA.

[0083] Incidentally, the OTA-C filter of Fig. 12 has a structure such that the amplifies OTA1, OTA2 and OTA3 are supplied with the bias voltages VGN and VGP from the common current compensation type bias circuit BIAS respectively, but the input voltage to the amplifier OTA3 is different in level from the input voltages to the amplifiers OTA1 and OTA2. As shown in Fig. 13, therefore, there are provided the different current compensation type bias circuits BIAS1 and BIAS2 for feeding the bias voltages VGN and VGP with respect to which the currents are compensated according to the respective input voltages, so that the distortion can be further reduced. In this case, the bias circuit BIAS2 is fed with the input of the OTA3. Moreover, the bias circuits BIAS, BIAS1 and BIAS2 of Figs. 12 and 13 have the same structure as that of the bias circuit BIAS of Fig. 5.

[0084] Fig. 16 shows a radio communication system as an application example of the filter circuit (low-pass filter) shown in Fig. 14.

[0085] In Fig. 16, reference numeral 50 designates a voice codec connected to a microphone MP and a speaker SPK for effecting conversions of an audio signal to an electric signal and of an analog signal to a digital signal; numeral 60 designates a channel codec circuit for performing timing sharing processing, for generating and checking error correcting codes and for forming and analyzing a transmission/reception frame; and numeral 70 designates a modem (modulating/ demodulating circuit) for modulating/demodulating a transmitted/received signal.

[0086] The voice codec 50 comprises low-pass filters 51 and 52, an A/D converter 53, a D/A converter 54, a coder 55 for compressing an input audio signal, and a decoder 56 for expanding an audio output. Moreover, the modem 70 comprises low-pass filters 71 and 72, a D/A converter 73, an A/D converter 74, a modulator 75 and a demodulator 76. The voice codec 50, channel codec circuit 60 and modem (modulator/demodulator) 70 are formed on one semiconductor chip and integrated into one semiconductor integrated circuit, although not especially limited thereto.

[0087] Incidentally, in Fig. 16, numeral 80 designates a high-frequency unit comprising of a power amplifier for transmission, a synthesizer for generating a carrier signal, and an adder for combining the carrier signal with the transmission/reception signal, and numeral 81 designates a transmitting/receiving antenna.

[0088] In this embodiment, as the low-pass filters 51 and 52, and 71 and 72, the filter circuits shown in Fig. 12 or 13 are used, and the voice codec 50 and the modem 70 have therein Gm control circuits which include Vc generators, as shown in Fig. 10, for generating the control voltages Vc to control the transconductances Gm of the OTAs (the Gm-controllable differential amplifiers) constituting the low-pass filters 51 and 52, and 71 and 72.

[0089] Moreover, the Gm control circuit in the voice codec 50 is provided commonly for the low-pass filters 51 and 52, and the Gm control circuit in the modem 70 is provided commonly for the low-pass filters 71 and 72. Since the ratios of the capacitive elements and the resistance elements on the same semiconductor chip can be set relatively accurate, the transconductances of the OTAs and the cut-off frequencies of the filter can be accurately controlled to constants even if the Gm-control circuits are commonly provided for a plurality of filter circuits on a single chip. Moreover, an increase in the occupied area can be suppressed by making the Gm control circuit common, as in the embodiment.

[0090] In the embodiments, as has been described above, the Gm-controllable amplifier used in an OTA-C filter has a structure that the constant voltage from the bias circuit is applied to the gates of the load MOSFETs connected to the drains of the input differential MOS-

FETs of the basic differential amplifier to cause the load MOSFETs to operate as constant current sources and the inverted output terminal of the circuit is connectd to the input terminals. As a result, the load MOSFETs of the input differential MOSFETs are made to serve as constant current sources so that the drain voltages of the input differential MOSFETs become independent of the threshold voltage of the load MOSFETs. Even if the supply voltage VDD is set to as low as about 1.5 V, the input differential MOSFETs can be prevented from being unsaturated when the input signals rise, providing a low-voltage amplifier. Since, moreover, the inverted output terminals are coupled to the input terminals, the currents outputted from the inverted output terminals and flowing in the direction opposite to that of the current from the non-inverted output terminals can be absorbed from the non-inverting input terminals, to produce an effect that the balance of the circuit can be easily held.

[0091] Moreover, the basic differential amplifier is equipped with a current compensation type bias generator for generating a bias voltage according to the level of an input voltage monitored, and feeding the bias voltage to the gates of the constant current MOSFETs of the basic differential amplifier so as to compensate the current fluctuation due to the channel length modulation effect. As a result, the bias current of the differential amplifier becomes constant to raise an effect that the transconductance can be stabilized and the output distortion can be reduced.

[0092] The OTA, as described in this specification, can be deemed as a circuit for converting the input differential voltage to a current. In short, the OTA can be deemed as a differential-voltage/current converter.

[0093] Although our invention has been specifically described in connection with its embodiments, it should not be limited thereto but is to be defined in accordance with the appended claims. Although in the foregoing embodiments, by the primary low-pass filter and the ternary low-pass filter are shown, the present invention can also be applied to a secondary low-pass filter and a quartic or higher order low-pass filter. Moreover, the present invention can be used in a band-pass filter or a high-pass filter.

[0094] The effects obtained by the representative of the inventions disclosed herein will be briefly described in the following.

[0095] It is possible to realize a filter circuit which operates on a low voltage with a low power consumption, and has a low distortion and a small frequency deviation.

[0096] The characteristics of the OTA-C filter circuit can be relatively greatly changed, for example, by changing the value of the capacitive element C shown in Fig. 2, by changing the sizes of the MOSFETs M1 to M5 of the OTA shown in Fig. 1, or by changing the both. In this case, the characteristics may be finely adjusted by changing the value of the control voltage Vc. In cases where the ease of the design is considered, it is preferable to change the value of the capacitive element C. The variation of the characteristics due to the production variation may naturally be adjusted by adjusting the control voltage Vc.

Claims

1. An analog filter circuit comprising:

   (i) a voltage/current conversion circuit having an inversion input node (IN^-), a non-inversion input node (IN^+) for receiving an input voltage signal, an inversion output node (OUT^-) and a non-inversion output node (OUT^+) coupled to the inversion input node,

   the inversion output node of the voltage/current conversion circuit being coupled to the non-inversion input node of the voltage/current conversion circuit, the voltage/current conversion circuit having a first differential MOSFET (M3, Q3) having a source, a drain providing a first output signal to the inversion output node and a gate, a second differential MOSFET (M4, Q4) having a source, a drain providing a second output signal to the non-inversion output node and a gate, a current source (M5, ICO) connected to the source of said first differential MOSFET (M3, Q3), a first current circuit (M1, IO) connected between a power supply terminal to which a predetermined voltage is applied and the drain of said first differential MOSFET (M3, Q3);

   and a second current circuit (M2, IO) connected between said power supply terminal and the drain of said second differential MOSFET (M4, Q4); and

   (ii) a capacitance circuit (C) connected to the non-inversion output node of said voltage/current conversion circuit; and **characterised in that**:

   (iii) a control circuit (MB0, MB1.....MBn) connected to the first current circuit (MI, IO) and the second current circuit (M2, IO) of said voltage/current conversion circuit, and used to determine the current values of the first and second current circuits (M1, IO; M2, IO); and wherein the gate of the first differential MOSFET (M3, Q3) receives a first input signal from the non-inversion input node, the gate of the second differential MOSFET (M4, Q4) receives a second input signal from the inversion input node, and the source of the first differential MOSFET (M3, Q3) is connected to the source of the second differential MOSFET (M4, Q4).

2. An analog filter circuit according to claim 1, wherein said first current circuit is a third MOSFET (M1) having a source-drain path connected between said

power terminal and the drain of said first MOSFET (M3), and a gate,

said second current circuit is a fourth MOSFET (M2) having a source-drain path connected between said power supply terminal and the drain of said second MOSFET (M4), and a gate, and

said control circuit (MB0, MB1.....MBn) is a bias circuit for changing the bias voltage applied to the gates of said third and fourth MOSFETs (M1, M2) in accordance with a control signal.

3. An analog filter circuit according to claim 1 or claim 2, wherein

said current source is a fifth MOSFET (M5) having a source-drain path connected between the source of said first MOSFET (M3) and a predetermined power supply terminal, and a gate, and

said control circuit (MB0, MB1.....MBn) includes a bias circuit for changing a bias voltage applied to the gate of said fifth MOSFET (M5) in accordance with said control signal.

4. An analogue filter circuit according to any one of the preceding claims, wherein

said control signal includes a signal corresponding to an input signal fed to the gate of said first MOSFET (M3), and

said bias circuit includes a compensation circuit for feeding the gates of said first and second MOSFETs (M3, M4) with a bias voltage which compensates the change in the source-drain currents of said first and second MOSFETs (M3, M4) with the change in the voltages at the drains of said first and second MOSFETs (M3, M4) due to the change in said input signal.

5. An analog filter circuit according to any one of claims 1 to 3, wherein

said control signal includes a signal corresponding to an input signal fed to the gate of said first MOSFET (M3), and

said bias circuit includes a first compensation circuit for feeding the gates of said first and second MOSFETs (M3, M4) with a bias voltage which compensates the change in the source-drain currents of said first and second MOSFETs (M3, M4) with the change in the voltages at the drains of said first and second MOSFETs (M3, M4) due to the change in said input signal; and a second compensation circuit (MB11) for feeding the gate of said fifth MOSFET (M5) with a bias voltage which compensates the change in the source-drain current of said fifth MOSFET (M5) with the change in the voltage at the drain of the fifth MOSFET (M5) due to the change in said input signal.

6. An analog filter circuit according to any one of the preceding claims, wherein

said current source is a sixth MOSFET (M6) having a source-drain path connected between the source of said first MOSFET (M3) and a predetermined power supply terminal, and a gate, and

said control circuit includes a bias circuit (MB21) for changing a bias voltage fed to the gate of said sixth MOSFET (M1) in accordance with said control signal.

7. An analog filter circuit according-to any one of the preceding claims

wherein said voltage/current conversion circuit includes,

a first output node for receiving an output signal from the drain of said first MOSFET (M3);

a second output node for receiving an output signal from the drain of said second MOSFET (M4) ;

a first input node for receiving a signal fed to the gate of said first MOSFET (M3);

and a second input node for receiving a signal fed to the gate of said second MOSFET (M4), and

wherein said capacitance circuit (C) is connected to said second output node, and said second input node is connected to said second output node.

8. An analog filter circuit formed on a setaiconductor substrate, comprising:

a plurality of voltage/current conversion circuits,

a plurality of capacitance circuits (C) connected to the respective non-inversion output nodes of said plurality of voltage/current conversion circuits; and

a control circuit (MB0, MB1.....MBn) is provided common to said plurality of voltage/current conversion circuits,

wherein each of said voltage/current conversion circuits includes:

an inversion input node (IN^-), a non-inversion input node (IN^+) for receiving an input voltage signal, an inversion output node (OUT^-) and a non-inversion output node (OUT^+) coupled to the inversion input node, the inversion output node of the voltage/current conversion circuit being coupled to the non-inversion input node of the voltage/current conversion circuit, and including:

a first differential MOSFET (M3, Q3) having a source, a drain providing a first output signal to the inversion output node and a gate;

a second differential MOSFET (M4, Q4) having a source, a drain providing a second output signal to the non-inversion out-

put node and a gate;
a current source (M5, ICO) connected to the source of said first differential MOSFET;
a first current circuit (M1, IO) connected between a power supply terminal to which a predetermined voltage is applied and the drain of said first differential MOSFET (M3, Q3); and
a second current circuit (M2, IO) connected between said power supply terminal and the drain of said second differential MOSFET (M4, Q1);

characterised in that:

a control circuit (MB0, MB1.....MBn) is provided common to said plurality of voltage/current conversion circuits, said control circuit (MB0, MB1.....MBn) is connected to the first and second current circuits (M1, IO; M2, IO) of each of said voltage/current conversion circuits, and used to determine the current values of the first and second current circuits; and
in each said voltage/current conversion circuit, the gate of the first differential MOSFET (M3, Q3) receives a first input signal from the non-inversion input node, the gate of the second differential MOSFET (M4, Q4) receives a second input signal from the inversion input node, and the source of the first differential MOSFET (M3, Q3) is connected to the source of the second differential MOSFET (M4, Q4).

9. An analog filter circuit according to claim 8, said first current circuit is a third MOSFET (M1) having a source-drain path connected between said power supply terminal and the drain of said first MOSFET (M3), and a gate,

said second current circuit is a fourth MOSFET (M2) having a source-drain path connected between said power supply terminal and the drain of said second MOSFET (M4), and a gate, and

said control circuit (MB0, MB1.....MBn) is a bias circuit for changing the bias voltage fed to the gate of said third and fourth MOSFETs in accordance with a control signal.

10. An analog filter circuit according to claim 9,

wherein

said current source is a fifth MOSFET (M5) having a source-drain path connected between the source of said first MOSFET (M3) and a predetermined power supply terminal, and a gate, and

said control circuit (MB0, MB1.....MBn) includes a bias circuit for changing a bias voltage fed to the gate of said fifth MOSFET (M5) in accordance with said control signal.

11. An analog filter circuit according to claim 1 formed on a single semiconductor substrate wherein said voltage/current conversion circuit includes:

a third differential MOSFET (Q1) having a source coupled to the source of the first differential MOSFET (Q3), a drain coupled to the drain of the second differential MOSFET (Q4) and a gate;
a fourth differential MOSFET (Q2) having a source coupled to the source of the first differential MOSFET (Q3), a drain coupled to the drain of the first differential MOSFET (Q3) and a gate;
a first level shift circuit (Q5, Q6) connected to the gates of said first and third differential MOSFETs (Q3, Q1);
a second level shift circuit (Q7, Q8) connected to the gates of said second and fourth differential MOSFETs (Q4, Q2)
a first level-up circuit (Q11, I1) for raising an input signal received, and feeding the level-up signal to said first level shift circuit (Q5, Q6); and
a second level-up circuit (Q12, I1) for raising an input signal received, and feeding the level-up signal to said second level shift circuit (Q7, Q8).

12. An analog filter circuit according to claim 11, wherein

said first level-up circuit (Q11, I1) includes a fifth MOSFET (Q11) for a source follower which receives said input signal;

said second level-up circuit (Q12 I1) includes a sixth MOSFET (Q12) for a source follower which receives said input signal;

said first level shift circuit includes seventh and eighth MOSFETs (Q5, Q6) having substantially the same characteristics as those of said fifth MOSFET (Q11), said seventh MOSFET (Q5) is diode-connected and feeds the output of said first level-up circuit to said first differential MOSFET (Q3), and said eighth MOSFET (Q6) is diode-connected and feeds the output of said first level-up circuit to said third differential MOSFET (Q4), and

said second level shift circuit includes ninth and tenth MOSFETs (Q7, Q8) having substantially the same characteristics as those of said sixth MOSFET (Q12), said ninth MOSFET (Q7) is diode-connected and feeds the output of said second level-up circuit to said second differential MOSFET (Q4), and said tenth MOSFET (Q8) is diode-connected and feeds the output of said second level-up circuit to said fourth differential MOSFET (Q2).

13. 'An analog filter circuit according to claim 12, wherein

said first level shift circuit further includes a variable current source connected to the sources of said seventh and eighth MOSFETs (Q5, Q6), and

said second level shift circuit further includes a variable current source connected to the sources of said ninth and tenth MOSFETs (Q7, Q8).

14. An analog filter circuit according to claim 11, wherein said analog filter circuit is a filter circuit built in an audio codec or modem.

15. A semiconductor integrated circuit device formed on a single semiconductor substrate and including a filter circuit, said device comprising:

a first filter circuit (20) according to claim 1 having a control terminal, coupled to the control circuit (MB0, MB1.....MBn), an input terminal formed by the non-inversion input node and an output terminal formed by the non-inversion output node and having characteristics changed by a voltage applied to said control terminal;

a phase difference detector (30) which receives a reference output signal (Vo) outputted from said first filter circuit (20) and a reference signal (Vi) having a predetermined frequency, when said reference signal is fed to the input terminal of said first filter circuit (20), and outputs a control signal (Vc) corresponding to the phase difference between said reference output signal (Vo) and said reference signal (Vi); and

a second filter circuit (10) according to claim 1 having a control terminal coupled to the control circuit (MB0, MB1.....MBn), an input terminal formed by the non-inversion input node and an output terminal formed by the non-inversion output node and having characteristics changed by a voltage fed to said control terminal,

wherein said control signal (Vc) output by said phase difference detector (30) is fed to the control terminals of said first and second filter circuits (10, 20), said second filter circuit (10) being used as said filter circuit.

16. A semiconductor integrated circuit device according to claim 15,

wherein said semiconductor integrated circuit device is an audio codec or modem.

17. An analog filter circuit according to claim 1,

wherein said analog filter circuit is a filter circuit built in an audio codec or modem.

Patentansprüche

1. Analogfilterschaltkreis umfassend:

(i) einen Spannungs/Stromumwandlungsschaltkreis mit einem Inversionseingangsknoten (IN-), einem Nicht-Inversionseingangsknoten (IN+) zum Empfangen eines Eingangsspannungssignals, einem Inversionsausgangsknoten (OUT-) und einem Nicht-Inversionsausgangsknoten (OUT+), der mit dem Inversionseingangsknoten verschaltet ist,

wobei der Inversionsausgangsknoten des Spannungs/Stromumwandlungsschaltkreises mit dem Nicht-Inversionseingangsknoten der Spannungs/Stromumwandlungsschaltkreises verschaltet ist, wobei der Spannungs/Stromumwandlungsschaltkreis

einen ersten differentiellen MOSFET (M3, Q3) mit einem Source-Anschluß, einem ein erstes Ausgangssignal für den Inversionsausgangsknoten zur Verfügung stellenden Drain-Anschluß und einem Gate-Anschluß,

einen zweiten differentiellen MOSFET (M4, Q4) mit einem Source-Anschluß, einem ein zweites Ausgangssignal für den Nicht-Inversionsausgangsknoten zur Verfügung stellenden Drain-Anschluß und einem Gate-Anschluß,

eine mit dem Source-Anschluß des ersten differentiellen MOSFETs (M3, Q3) verschaltete Stromquelle (M5, ICO),

einen zwischen einen Stromversorgungsanschluß, an den eine vorbestimmte Spannung angelegt wird, und den Drain-Anschluß des ersten differentiellen MOSFETs (M3, Q3) geschalteten ersten Strom-Schaltkreis (M1, IO); und

einen zwischen den Stromversorgungsanschluß und den Drain-Anschluß des zweiten differentiellen MOSFETs (M4, Q4) geschalteten zweiten Strom-Schaltkreis (M2, IO) aufweist; und

(ii) einen mit dem Nicht-Inversionsausgangsknoten des Strom/Spannungsumwandlungsschaltkreises verschalteten Kapazitätsschaltkreis (C); **gekennzeichnet durch**

(iii) einen mit dem ersten Strom-Schaltkreis (M1, IO) und dem zweiten Strom-Schaltkreis (M2, IO) des Spannungs/Stromumwandlungsschaltkreises verschalteten Steuerschaltkreis (MB0, MB1... MBn) zum Bestimmen der Stromwerte des ersten und des zweiten Strom-Schaltkreises (M1, IO; M2, IO), wobei der Gate-Anschluß des ersten differentiellen MOSFETs (M3, Q3) ein erstes Eingangssignal von dem Nicht-Inversionseingangsknoten empfängt, wobei der Gate-Anschluß des zweiten differen-

tiellen MOSFETs (M4, Q4) ein zweites Eingangssignal von dem Inversionseingangsknoten empfängt und

wobei der Source-Anschluß des ersten differentiellen MOSFETs (M3, Q3) mit dem Source-Anschluß des zweiten differentiellen MOSFETs (M4, Q4) verschaltet ist.

2. Schaltkreis nach Anspruch 1, wobei der erste Strom-Schaltkreis ein dritter MOSFET (M1) mit einem zwischen den Stromanschluß und den Drain-Anschluß des ersten MOSFETs (M3) geschalteten Source-Drain-Pfad und einem Gate-Anschluß ist,

wobei der zweite Strom-Schaltkreis ein vierter MOSFET (M2) mit einem zwischen den Stromversorgungsanschluß und den Drain-Anschluß des zweiten MOSFETs (M4) geschalteten Source-Drain-Pfad und einem Gate-Anschluß ist, und

wobei der Steuerschaltkreis (MB0, MB1... MBn) ein Vorspannungsschaltkreis zum Ändern der Vorspannung, die an den Gate-Anschlüssen des dritten und des vierten MOSFETs (M1, M2) anliegt, in Übereinstimmung mit einem Steuersignal ist.

3. Schaltkreis nach Anspruch 1 oder 2, wobei die Stromquelle ein fünfter MOSFET (M5) mit einem zwischen den Source-Anschluß des ersten MOSFETs (M3) und einen vorbestimmten Stromversorgungsanschluß geschalteten Source-Drain-Pfad und einem Gate-Anschluß ist, und

wobei der Steuerschaltkreis (MB0, MB1... MBn) einen Vorspannungsschaltkreis zum Ändern der Vorspannung, die an dem Gate-Anschluß des fünften MOSFETs (M5) anliegt, in Übereinstimmung mit dem Steuersignal beinhaltet.

4. Schaltkreis nach einem der vorhergehenden Ansprüche, wobei das Steuersignal ein Signal beinhaltet, das einem am Gate-Anschluß des ersten MOSFETs (M3) eingespeisten Eingangssignal zugehört, und

wobei der Vorspannungsschaltkreis einen Kompensationsschaltkreis zum Speisen der Gate-Anschlüsse des ersten und des zweiten MOSFETs (M3, M4) mit einer Vorspannung, die die Änderung in den Source-Drain-Strömen des ersten und des zweiten MOSFETs (M3, M4) durch die Änderung in den Spannungen an den Drain-Anschlüssen des ersten und des zweiten MOSFETs (M3, M4) aufgrund der Änderung im Eingangssignal kompensiert, beinhaltet.

5. Schaltkreis nach einem der Ansprüche 1 bis 3, wobei das Steuersignal ein Signal beinhaltet, das zu einem am Gate-Anschluß des ersten MOSFETs (M3) eingespeisten Eingangssignal gehört, und

wobei der Vorspannungsschaltkreis einen ersten Kompensationsschaltkreis zum Speisen der Gate-Anschlüsse des ersten und des zweiten MOSFETs (M3, M4) mit einer Vorspannung, die die Änderung in den Source-Drain-Strömen des ersten und des zweiten MOSFETs (M3, M4) durch die Änderung in den Spannungen an den Drain-Anschlüssen des ersten und des zweiten MOSFETs (M3, M4) aufgrund der Änderung im Eingangssignal kompensiert, und einen zweiten Kompensationsschaltkreis (MB11) zum Speisen des Gate-Anschlusses des fünften MOSFETs (M5) mit einer Vorspannung, die die Änderung im Source-Drain-Strom des fünften MOSFETs (M5) durch die Änderung in der Spannung am Drain-Anschluß des fünften MOSFETs (M5) aufgrund der Änderung im Eingangssignal kompensiert, beinhaltet.

6. Schaltkreis nach einem der vorhergehenden Ansprüche, wobei die Stromquelle ein sechster MOSFET (M6) mit einem zwischen dem Source-Anschluß des ersten MOSFETs (M3) und einem vorbestimmten Stromversorgungsanschluß geschalteten Source-Drain-Pfad und einem Gate-Anschluß ist, und

wobei der Steuerschaltkreis einen Vorspannungsschaltkreis (MB21) zum Ändern einer am Gate-Anschluß des sechsten MOSFETs (M1) eingespeisten Vorspannung in Übereinstimmung mit dem Steuersignal beinhaltet.

7. Schaltkreis nach einem der vorhergehenden Ansprüche, wobei der Spannungs/Stromumwandlungsschaltkreis beinhaltet:

einen ersten Ausgangsknoten zum Empfangen eines Ausgangssignals vom Drain-Anschluß des ersten MOSFETs (M3);
einen zweiten Ausgangsknoten zum Empfangen eines Ausgangssignals vom Drain-Anschluß des zweiten MOSFETs (M4);
einen ersten Eingangsknoten zum Empfangen eines am Gate-Anschluß des ersten MOSFETs (M3) eingespeisten Signals;
einen zweiten Eingangsknoten zum Empfangen eines am Gate-Anschluß des zweiten MOSFETs (M4) eingespeisten Signals,

wobei der Kapazitätsschaltkreis (C) mit dem zweiten Ausgangsknoten, und der zweite Eingangsknoten mit dem zweiten Ausgangsknoten verschaltet ist.

8. Analogfilterschaltkreis, ausgebildet auf einem Halbleitersubstrat und umfassend:

eine Vielzahl von Spannungs/Stromumwandlungsschaltkreisen,
eine Vielzahl von mit den jeweiligen Nicht-In-

versionsausgangsknoten der Vielzahl von Strom/Spannungsumwandlungsschaltkreisen verschalteten Kapazitätsschaltkreisen (C); und einen gemeinsam für die Vielzahl von Strom/Spannungsumwandlungsschaltkreisen zur Verfügung gestellten Steuerschaltkreis (MB0, MB1...MBn),

wobei ein jeweiliger Spannungs/Stromumwandlungsschaltkreis beinhaltet:

einen Inversionseingangsknoten (IN-), einen Nicht-Inversionseingangsknoten (IN+) zum Empfangen eines Eingangsspannungssignals, einen Inversionsausgangsknoten (OUT-) und einen Nicht-Inversionsausgangsknoten (OUT+), der mit dem Inversionseingangsknoten verschaltet ist, wobei der Inversionsausgangsknoten des Spannungs/Stromumwandlungsschaltkreises mit dem Nicht-Inversionseingangsknoten des Spannungs/Stromumwandlungsschaltkreises verschaltet ist,

und beinhaltet:

einen ersten differentiellen MOSFET (M3, Q3) mit einem Source-Anschluß, einem dem Inversionsausgangsknoten ein erstes Ausgangssignal zur Verfügung stellenden Drain-Anschluß und einem Gate-Anschluß;

einen zweiten differentiellen MOSFET (M4, Q4) mit einem Source-Anschluß, einem dem Nicht-Inversionsausgangsknoten ein zweites Ausgangssignal zur Verfügung stellenden Drain-Anschluß und einem Gate-Anschluß;

eine mit dem Source-Anschluß des ersten differentiellen MOSFETs verschaltete Stromquelle (M5, IC0);

einen zwischen einen Stromversorgungsanschluß, an den eine vorbestimmte Spannung angelegt wird, und den Drain-Anschluß des ersten differentiellen MOSFETs (M3, Q3) geschalteten ersten Strom-Schaltkreis (M1, I0); und

einen zwischen den Stromversorgungsanschluß und den Drain-Anschluß des zweiten differentiellen MOSFETs (M4, Q1) geschalteten zweiten Strom-Schaltkreis (M2, I0);

dadurch gekennzeichnet, daß

ein Steuerschaltkreis (MB0, MB1...MBn) gemeinsam für die Vielzahl von Spannungs/Stromumwandlungsschaltkreisen zur Verfügung gestellt ist, wobei der Steuerschaltkreis (MB0, MB1... MBn) mit dem ersten und dem zweiten Stromschaltkreis (M1, I0; M2, I0) eines jeweiligen Spannungs/Stromumwandlungsschaltkreises verschaltet ist, um die Stromwerte des ersten und des zweiten Stromschaltkreises zu bestimmen; und

wobei in einem jeweiligen Spannungs/Stromumwandlungsschaltkreis der Gate-Anschluß des ersten differentiellen MOSFETs (M3, Q3) ein erstes Eingangssignal von dem Nicht-Inversionseingangsknoten erhält, der Gate-Anschluß des zweiten differentiellen MOSFETs (M4, Q4) ein zweites Eingangssignal von dem Inversionseingangsknoten empfängt und der Source-Anschluß des ersten differentiellen MOSFETs (M3, Q3) mit dem Source-Anschluß des zweiten differentiellen MOSFETs (M4, Q4) verschaltet ist.

9. Schaltkreis nach Anspruch 8, wobei der erste Strom-Schaltkreis ein dritter MOSFET (M1) mit einem zwischen den Stromversorgungsanschluß und den Drain-Anschluß des ersten MOSFETs (M3) geschalteten Source-Drain-Pfad und einem Gate-Anschluß ist,

wobei der zweite Strom-Schaltkreis ein vierter MOSFET (M2) mit einem zwischen den Stromversorgungsanschluß und den Drain-Anschluß des zweiten MOSFETs (M4) geschalteten Source-Drain-Pfad und einem Gate-Anschluß ist, und

wobei der Steuerschaltkreis (MB0, MB1..... MBn) ein Vorspannungsschaltkreis zum Ändern der am Gate-Anschluß des dritten und des vierten MOSFETs eingespeisten Vorspannung in Übereinstimmung mit einem Steuersignal ist.

10. Schaltkreis nach Anspruch 9, wobei die Stromquelle ein fünfter MOSFET (M5) mit einem zwischen den Source-Anschluß des ersten MOSFETs (M3) und einen vorbestimmten Stormversorgungsanschluß geschalteten Source-Drain-Pfad und einem Gate-Anschluß ist und

wobei der Steuerschaltkreis (MB0, MB1..... MBn) einen Vorspannungsschaltkreis zum Ändern einer am Gate-Anschluß des fünften MOSFETs (M5) eingespeisten Vorspannung in Übereinstimmung mit dem Steuersignal beinhaltet.

11. Schaltkreis nach Anspruch 1, ausgebildet auf einem einzelnen Halbleitersubstrat, wobei der Spannungs/Stromumwandlungsschaltkreis beinhaltet:

einen dritten differentiellen MOSFET (Q1) mit einem mit dem Source-Anschluß des ersten differentiellen MOSFETs (Q3) verschalteten Source-Anschluß, einem mit dem Drain-Anschluß des zweiten differentiellen MOSFETs (Q4) verschalteten Drain-Anschluß und einem Gate-Anschluß;

einen vierten differentiellen MOSFET (Q2) mit einem mit dem Source-Anschluß des ersten differentiellen MOSFETs (Q3) verschalteten Source-Anschluß, einem mit dem Drain-Anschluß des ersten differentiellen MOSFETs (Q3) verschalteten Drain-Anschluß und einem Gate-Anschluß;

einen ersten Pegelverschiebungsschaltkreis

(Q5, Q6), der mit den Gate-Anschlüssen des ersten und des dritten differentiellen MOSFETs (Q3, Q1) verschaltet ist;
einen zweiten Pegelverschiebungsschaltkreis (Q7, Q8), der mit den Gate-Anschlüssen des zweiten und des vierten differentiellen MOSFETs (Q4, Q2) verschaltet ist;
einen ersten Pegelerhöhungschaltkreis (Q11, I1) zum Erhöhen eines empfangenen Eingangssignals und zum Einspeisen des Pegelerhöhungssignals am ersten Pegelverschiebungsschaltkreis (Q5, Q6); und
einen zweiten Pegelerhöhungschaltkreis (Q12, I1) zum Erhöhen eines empfangenen Eingangssignals und zum Einspeisen des Pegelerhöhungssignals am zweiten Pegelverschiebungsschaltkreis (Q7, Q8).

12. Schaltkreis nach Anspruch 11, wobei der erste Pegelerhöhungschaltkreis (Q11, I1) einen fünften MOSFET (Q11) für einen Sourcefolger beinhaltet, der das Eingangssignal empfängt;

der zweite Pegelerhöhungschaltkreis (Q12, I1) einen sechsten MOSFET (Q12) für einen Sourcefolger beinhaltet, der ein Eingangssignal empfängt;

wobei der erste Pegelverschiebungsschaltkreis einen siebten und einen achten MOSFET (Q5, Q6) mit im wesentlichen gleichen Charakteristika wie denen des fünften MOSFETs (Q11) beinhaltet, wobei der siebte MOSFET (Q5) diodengeschaltet ist und die Ausgabe des ersten Pegelerhöhungsschaltkreises dem ersten differentiellen MOSFETs (Q3) einspeist, und wobei der achte MOSFET (Q6) diodengeschaltet ist und die Ausgabe des ersten Pegelerhöhungsschaltkreises dem dritten differentiellen MOSFET (Q4) einspeist und

wobei der zweite Pegelverschiebungsschaltkreis einen neunten und einen zehnten MOSFET (Q7, Q8) mit im wesentlichen gleichen Charakteristika wie denen des sechsten MOSFETs (Q12) beinhaltet, wobei der neunte MOSFET (Q7) diodengeschaltet ist und die Ausgabe des zweiten Pegelerhöhungsschaltkreises dem zweiten differentiellen MOSFET (Q4) einspeist, und wobei der zehnte MOSFET (Q8) diodengeschaltet ist und die Ausgabe des zweiten Pegelerhöhungsschaltkreises dem vierten differentiellen MOSFET (Q2) einspeist.

13. Schaltkreis nach Anspruch 12, wobei der erste Pegelverschiebungsschaltkreis weiterhin eine mit den Source-Anschlüssen des siebten und des achten MOSFETs (Q5, Q6) verschaltete variable Stromquelle beinhaltet, und

wobei der zweite Pegelverschiebungsschaltkreis weiterhin eine mit den Source-Anschlüssen des neunten und des zehnten MOSFETs (Q7, Q8) verschaltete variable Stromquelle beinhaltet.

14. Schaltkreis nach Anspruch 11, wobei der Analogfilterschaltkreis in einen Audiocodec oder ein Modem eingebaut ist.

15. Integrierte Halbleiter-Schaltkreisvorrichtung, ausgebildet auf einem einzelnen Halbleitersubstrat und beinhaltend einen Filterschaltkreis, wobei die Vorrichtung umfaßt:

einen ersten Filterschaltkreis (20) nach Anspruch 1 mit einem Steueranschluß, der mit dem Steuerschaltkreis (MB0, MB1.....MBn) verschaltet ist, einem durch den Nicht-Inversionseingangsknoten ausgebildeten Eingangsanschluß und einem durch den Nicht-Inversionsausgangsknoten ausgebildeten Ausgangsanschluß, wobei die Charakteristiken durch eine an dem Steueranschluß angelegte Spannung änderbar sind;
einen Phasendifferenzdetektor (30), der ein von dem ersten Filterschaltkreis (20) ausgegebenes Referenzausgangssignal (Vo) und ein Referenzsignal (Vi) mit einer vorbestimmten Frequenz empfängt, wenn das Referenzsignal am Eingangsanschluß des ersten Filterschaltkreises (20) eingespeist ist, und der ein der Phasendifferenz zwischen dem Referenzausgangssignal (Vo) und dem Referenzsignal (Vi) entsprechendes Steuersignal (Vc) ausgibt; und
einen zweiten Filterschaltkreis (10) nach Anspruch 1 mit einem mit dem Steuerschaltkreis (MB0, MB1.....MBn) verschalteten Steueranschluß, einem durch den Nicht-Inversionseingangsknoten ausgebildeten Eingangsanschluß und einem durch den Nicht-Inversionsausgangsknoten ausgebildeten Ausgangsanschluß, wobei die Charakteristiken durch eine am Steueranschluß angelegte Spannung änderbar sind,

wobei das durch den Phasendifferenzdetektor (30) ausgegebene Steuersignal (Vc) den Steueranschlüssen des ersten und des zweiten Filterschaltkreises (10, 20) eingespeist ist, wobei der zweite Filterschaltkreises (10) als besagter Filterschaltkreis genutzt ist.

16. Vorrichtung nach Anspruch 15, wobei die Vorrichtung ein Audiocodec oder Modem ist.

17. Schaltkreis nach Anspruch 1, der in einen Audiocodec oder ein Modem eingebaut ist.

Revendications

1. Circuit de filtrage analogique comportant :

(i) un circuit de conversion tension/courant ayant un noeud d'entrée d'inversion (IN^-), un noeud d'entrée de non-inversion (IN^+) pour recevoir un signal de tension d'entrée, un noeud de sortie d'inversion (OUT^-) et un noeud de sortie de non-inversion (OUT^+) relié au noeud d'entrée d'inversion,

le noeud de sortie d'inversion du circuit de conversion tension/courant étant relié au noeud d'entrée de non-inversion du circuit de conversion tension/courant, le circuit de conversion tension/courant ayant un premier transistor métal-oxyde à effet de champ (MOSFET) différentiel (M3, Q3) ayant une source, un drain fournissant un premier signal de sortie au noeud de sortie d'inversion et une grille, un deuxième MOSFET différentiel (M4, Q4) ayant une source, un drain fournissant un second signal de sortie au noeud de sortie de non-inversion et une grille, une source de courant (M5, ICO) reliée à la source dudit premier MOSFET différentiel (M3, Q3), un premier circuit électrique (M_1, IO) monté entre une borne d'alimentation à laquelle est appliquée une tension prédéterminée et le drain dudit premier MOSFET différentiel (M3, Q3),

et un second circuit électrique (M2, IO) monté entre ladite borne d'alimentation et ledit drain dudit deuxième MOSFET différentiel (M4, Q4), et

(ii) un circuit capacitif (C) relié au noeud de sortie de non-inversion dudit circuit de conversion tension/courant, et **caractérisé en ce que** :

(iii) un circuit de commande (MB0, MB1 ... MBn) est relié au premier circuit électrique (MI, IO) et au second circuit électrique (M2, IO) dudit circuit de conversion tension/courant, et utilisé pour déterminer les valeurs du courant des premier et second circuits électriques (M1, IO ; M2, IO), et dans lequel la grille du premier MOSFET différentiel (M3, Q3) reçoit un premier signal d'entrée provenant du noeud d'entrée de non-inversion, la grille du deuxième MOSFET différentiel (M4, Q4) reçoit un second signal d'entrée provenant du noeud d'entrée d'inversion, et la source du premier MOSFET différentiel (M3, Q3) est reliée à la source du deuxième MOSFET différentiel (M4, Q4).

2. Circuit de filtrage analogique selon la revendication 1, dans lequel ledit premier circuit électrique est un troisième MOSFET (M1) ayant un trajet source-drain relié entre ladite borne d'alimentation et le drain dudit premier MOSFET (M3), et une grille,

ledit second circuit électrique est un quatrième MOSFET (M2) ayant un trajet source-drain relié entre ladite borne d'alimentation et le drain dudit deuxième MOSFET (M4), et une grille, et

ledit circuit de commande (MB0, MB1 ... MBn) est un circuit de polarisation permettant de changer la tension de polarisation appliquée aux grilles desdits troisième et quatrième MOSFET (M1, M2) conformément à un signal de commande.

3. Circuit de filtrage analogique selon la revendication 1 ou la revendication 2, dans lequel

ladite source de courant est un cinquième MOSFET (M5) ayant un trajet source-drain relié entre la source dudit premier MOSFET (M3) et une borne d'alimentation prédéterminée, et une grille, et

ledit circuit de commande (MB0, MB1 ... MBn) inclut un circuit de polarisation permettant de changer une tension de polarisation appliquée à la grille dudit cinquième MOSFET (M5) conformément audit signal de commande.

4. Circuit de filtrage analogique selon l'une quelconque des revendications précédentes, dans lequel

ledit signal de commande inclut un signal correspondant à un signal d'entrée appliqué à la grille dudit premier MOSFET (M3), et

ledit circuit de polarisation inclut un circuit de compensation pour appliquer aux grilles desdits premier et deuxième MOSFET (M3, M4) une tension de polarisation qui compense le changement des courants source-drain desdits premier et deuxième MOSFET (M3, M4) à l'aide du changement des tensions au niveau des drains desdits premier et deuxième MOSFET (M3, M4) dû au changement dudit signal d'entrée.

5. Circuit de filtrage analogique selon l'une quelconque des revendications 1 à 3, dans lequel

ledit signal de commande inclut un signal correspondant à un signal d'entrée appliqué à la grille dudit premier MOSFET (M3), et

ledit circuit de polarisation inclut un premier circuit de compensation pour appliquer aux grilles desdits premier et deuxième MOSFET (M3, M4) une tension de polarisation qui compense le changement des courants source-drain desdits premier et deuxième MOSFET (M3, M4) à l'aide du changement des tensions au niveau des drains desdits premier et deuxième MOSFET (M3, M4) dû au changement dudit signal d'entrée, et un second circuit de compensation (MB11) pour appliquer à la grille dudit cinquième MOSFET (M5) une tension de polarisation qui compense le changement du courant source-drain dudit cinquième MOSFET (M5) à l'aide du changement de la tension au niveau du drain du cinquième MOSFET (M5) dû au changement dudit signal d'entrée.

6. Circuit de filtrage analogique selon l'une quelconque des revendications précédentes, dans lequel

ladite source de courant est un sixième MOS-

FET (M6) ayant un trajet source-drain relié entre la source dudit premier MOSFET (M3) et une borne d'alimentation prédéterminée, et une grille, et

ledit circuit de commande inclut un circuit de polarisation (MB21) permettant de changer une tension de polarisation appliquée à la grille dudit sixième MOSFET (M1) conformément audit signal de commande.

7. Circuit de filtrage analogique selon l'une quelconque des revendications précédentes,

dans lequel ledit circuit de conversion tension/courant inclut,

un premier noeud de sortie pour recevoir un signal de sortie provenant du drain dudit premier MOSFET (M3),

un second noeud de sortie pour recevoir un signal de sortie à partir du drain dudit deuxième MOSFET (M4),

un premier noeud d'entrée pour recevoir un signal appliqué à la grille dudit premier MOSFET (M3),

et un second noeud d'entrée pour recevoir un signal appliqué à la grille dudit deuxième MOSFET (M4), et

dans lequel ledit circuit de capacité (C) est relié audit second noeud de sortie, et ledit second noeud d'entrée est relié audit second noeud de sortie.

8. Circuit de filtrage analogique formé sur un substrat à semi-conducteurs, comportant :

une pluralité de circuits de conversion tension/courant,

une pluralité de circuits capacitifs (C) reliés aux noeuds de sortie de non-inversion respectifs de ladite pluralité de circuits de conversion tension/courant, et

un circuit de commande (MB0, MB1 ... MBn) est fourni de manière commune à ladite pluralité de circuits de conversion tension/courant, et

dans lequel chacun desdits circuits de conversion tension/courant inclut :

un noeud d'entrée d'inversion (IN^-), un noeud d'entrée de non-inversion (IN^+) pour recevoir un signal de tension d'entrée, un noeud de sortie d'inversion(OUT^-) et un noeud de sortie de non-inversion (OUT^+) relié au noeud d'entrée d'inversion, le noeud de sortie d'inversion du circuit de conversion tension/courant étant relié au noeud d'entrée de non-inversion du circuit de conversion tension/courant, et incluant :

un premier MOSFET différentiel (M3, Q3) ayant une source, un drain fournissant un premier signal de sortie au noeud de sortie d'inversion et une grille,

un deuxième MOSFET différentiel (M4, Q4) ayant une source, un drain fournissant un second signal de sortie au noeud de sortie de non-inversion et une grille,

une source de courant (M5, ICO) reliée à la source dudit premier MOSFET différentiel,

un premier circuit électrique (M1, IO) relié entre une borne d'alimentation à laquelle est appliquée une tension prédéterminée et le drain dudit premier MOSFET différentiel (M3, Q3), et

un second circuit électrique (M2, IO) relié entre ladite borne d'alimentation et le drain dudit deuxième MOSFET différentiel (M4, Q1),

caractérisé en ce que :

un circuit de commande (MB0, MB1 ... MBn) est fourni de manière commune à ladite pluralité de circuits de conversion tension/courant, ledit circuit de commande (MB0, MB1 ... MBn) est relié auxdits premier et second circuits électriques (M1, I0 ; M2, IO) de chacun desdits circuits de conversion tension/courant, et utilisé pour déterminer les valeurs de courant des premier et second circuits électriques, et

dans chacun desdits circuits de conversion tension/courant, la grille du premier MOSFET différentiel (M3, Q3) reçoit un premier signal d'entrée provenant du noeud d'entrée de non-inversion, la grille du deuxième MOSFET différentiel (M4, Q4) reçoit un second signal d'entrée provenant du noeud d'entrée d'inversion, et la source du premier MOSFET différentiel (M3, Q3) est reliée à la source du deuxième MOSFET différentiel (M4, Q4).

9. Circuit de filtrage analogique selon la revendication 8, dans lequel

ledit premier circuit électrique est un troisième MOSFET (M1) ayant un trajet source-drain relié entre ladite borne d'alimentation et le drain dudit premier MOSFET (M3) et une grille,

ledit second circuit électrique est un quatrième MOSFET (M2) ayant un trajet source-drain relié entre ladite borne d'alimentation et le drain dudit deuxième MOSFET (M4), et une grille, et

ledit circuit de commande (MB0, MB1 ... MBn) est un circuit de polarisation permettant de changer la tension de polarisation appliquée à la grille desdits troisième et quatrième MOSFET conformément à un signal de commande.

10. Circuit de filtrage analogique selon la revendication 9,

dans lequel

ladite source de courant est un cinquième MOSFET (M5) ayant un trajet source-drain relié entre la source dudit premier MOSFET (M3) et une borne d'alimentation prédéterminée, et une grille, et

ledit circuit de commande (MB0, MB1 ... MBn) inclut un circuit de polarisation permettant de changer une tension de polarisation appliquée à la grille dudit cinquième MOSFET (M5) conformément audit signal de commande.

11. Circuit de filtrage analogique selon la revendication 1, formé sur un substrat à semi-conducteurs unique dans lequel ledit circuit de conversion tension/courant inclut :

un troisième MOSFET différentiel (Q1) ayant une source reliée à la source du premier MOSFET différentiel (Q3), un drain relié au drain du deuxième MOSFET différentiel (Q4) et une grille,

un quatrième MOSFET différentiel (Q2) ayant une source reliée à la source du premier MOSFET différentiel (Q3), un drain relié au drain du premier MOSFET différentiel (Q3) et une grille,

un premier circuit de décalage de niveau (Q5, Q6) relié aux grilles desdits premier et troisième MOSFET différentiels (Q3, Q1),

un second circuit de décalage de niveau (Q7, Q8) relié aux grilles desdits deuxième et quatrième MOSFET différentiels (Q4, Q2),

un premier circuit d'élévation de niveau (Q11, I1) pour augmenter un signal d'entrée reçu, et appliquer le signal d'élévation de niveau audit premier circuit de décalage de niveau (Q5, Q6), et

un second circuit d'élévation de niveau (Q12, I1) pour augmenter un signal d'entrée reçu, et appliquer le signal d'élévation de niveau audit second circuit de décalage de niveau (Q7, Q8).

12. Circuit de filtrage analogique selon la revendication 11, dans lequel

ledit premier circuit d'élévation de niveau (Q11, I1) inclut un cinquième MOSFET (Q11) pour un suiveur de source qui reçoit ledit signal d'entrée,

ledit second circuit d'élévation de niveau (Q12, I1) inclut un sixième MOSFET (Q12) pour un suiveur de source qui reçoit ledit signal d'entrée,

ledit premier circuit de décalage de niveau inclut un septième et un huitième MOSFET (Q5, Q6) ayant essentiellement les mêmes caractéristiques que celles dudit cinquième MOSFET (Q11), ledit septième MOSFET (Q5) est monté en diode et applique la sortie dudit premier circuit d'élévation de niveau audit premier MOSFET différentiel (Q3), et ledit huitième MOSFET (Q6) est monté en diode et applique la sortie dudit premier circuit d'élévation de niveau audit troisième MOSFET différentiel (Q4), et

ledit second circuit de décalage de niveau inclut un neuvième et un dixième MOSFET (Q7, Q8) ayant essentiellement les mêmes caractéristiques que celles dudit sixième MOSFET (Q12), ledit neuvième MOSFET (Q7) est monté en diode et applique la sortie dudit second circuit d'élévation de niveau audit deuxième MOSFET différentiel (Q4), et ledit dixième MOSFET (Q8) est monté en diode et applique la sortie dudit second circuit d'élévation de niveau audit quatrième MOSFET différentiel (Q2).

13. Circuit de filtrage analogique selon la revendication 12, dans lequel

ledit premier circuit de décalage de niveau inclut en outre une source de courant variable reliée aux sources desdits septième et huitième MOSFET (Q5, Q6), et

ledit second circuit de décalage de niveau inclut en outre une source de courant variable reliée aux sources desdits neuvième et dixième MOSFET (Q7, Q8).

14. Circuit de filtrage analogique selon la revendication 11, dans lequel ledit circuit de filtrage analogique est un circuit de filtrage monté dans un codeur-décodeur audio ou un modem.

15. Dispositif de circuit intégré à semi-conducteurs formé sur un substrat à semi-conducteurs unique et incluant un circuit de filtrage, ledit dispositif comportant :

un premier circuit de filtrage (20) selon la revendication 1, ayant une borne de commande, reliée au circuit de commande (MB0, MB1 ... MBn), une borne d'entrée formée par le noeud d'entrée de non-inversion et une borne de sortie formée par le noeud de sortie de non-inversion et ayant des caractéristiques changées par une tension appliquée à ladite borne de commande,

un détecteur de différence de phase (30) qui reçoit un signal de sortie de référence (Vo) délivré en sortie par ledit premier circuit de filtrage (20) et un signal de référence (Vi) ayant une fréquence prédéterminée, lorsque ledit signal de référence est appliqué à la borne d'entrée dudit premier circuit de filtrage (20), et délivre en sortie un signal de commande (Vc) correspondant à la différence de phase entre ledit signal de sortie de référence (Vo) et ledit signal de référence (Vi), et

un second circuit de filtrage (10) selon la revendication 1, ayant une borne de commande re-

FIG. 1

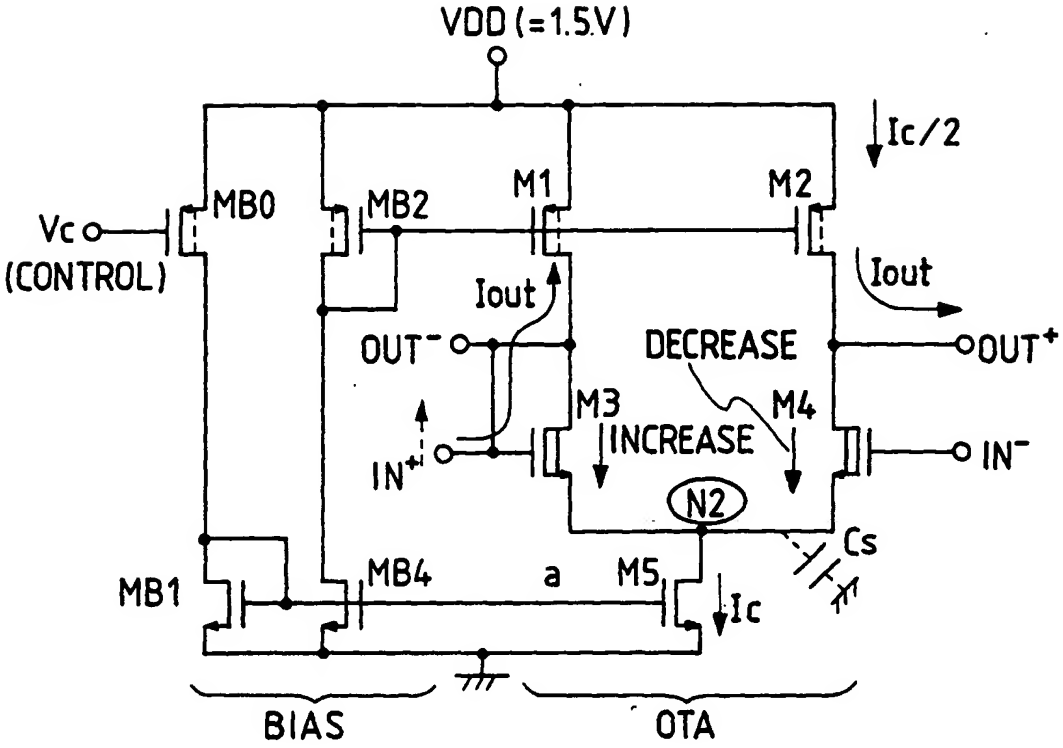

VDD (=1.5V)
Ic/2
MB0
MB2
M1
M2
Vc
(CONTROL)
Iout
Iout
OUT⁻
DECREASE
OUT⁺
M3
M4
INCREASE
IN⁺
IN⁻
N2
Cs
MB1
MB4
a
M5
Ic
BIAS
OTA

FIG. 2

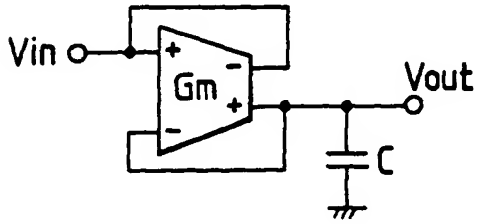
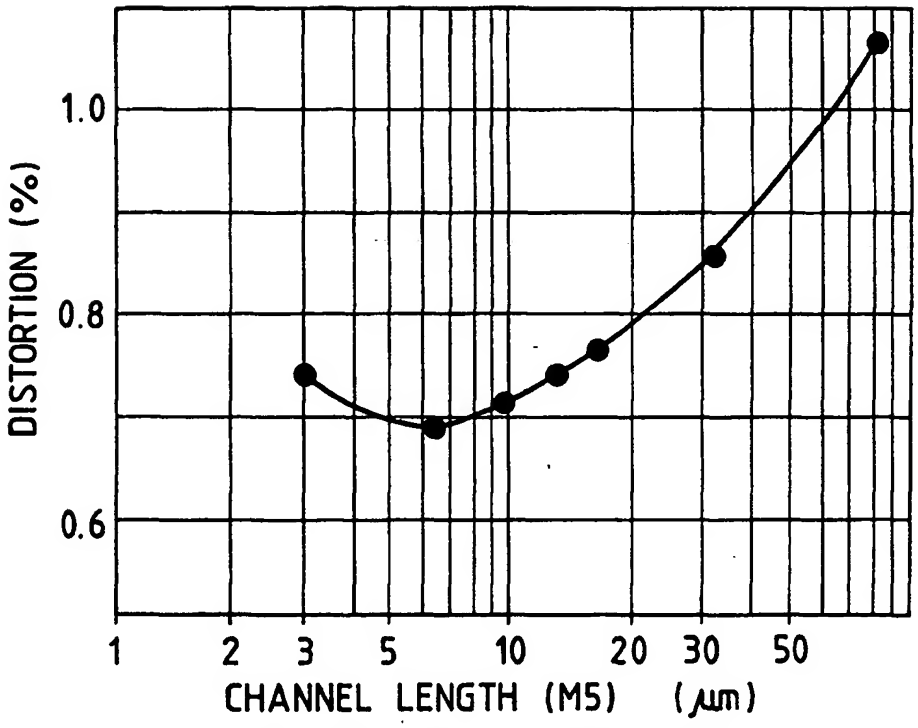

Vin
Gm
Vout
C

FIG. 3



DEPENDENCY OF DISTORTION ON CHANNEL LENGTH

FIG. 4

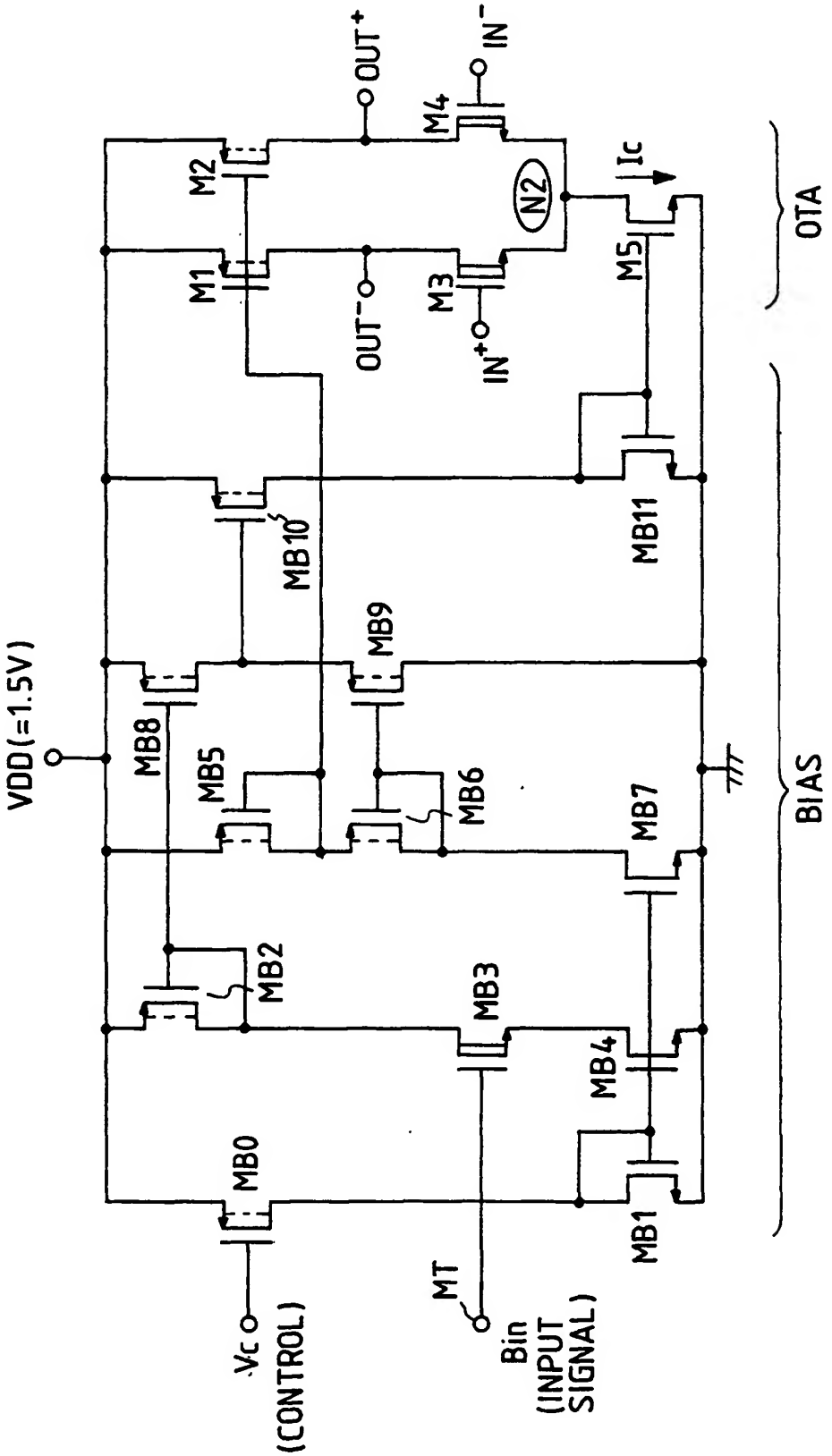

VDD(=1.5V)
OUT+
IN-
M4
M2
M1
OUT-
M3
IN+
N2
Ic
M5
OTA
MB10
MB11
MB9
MB8
MB5
MB6
MB7
BIAS
MB2
MB3
MB4
MB0
MB1
MT
Vc
(CONTROL)
Bin
(INPUT
SIGNAL)

FIG. 5

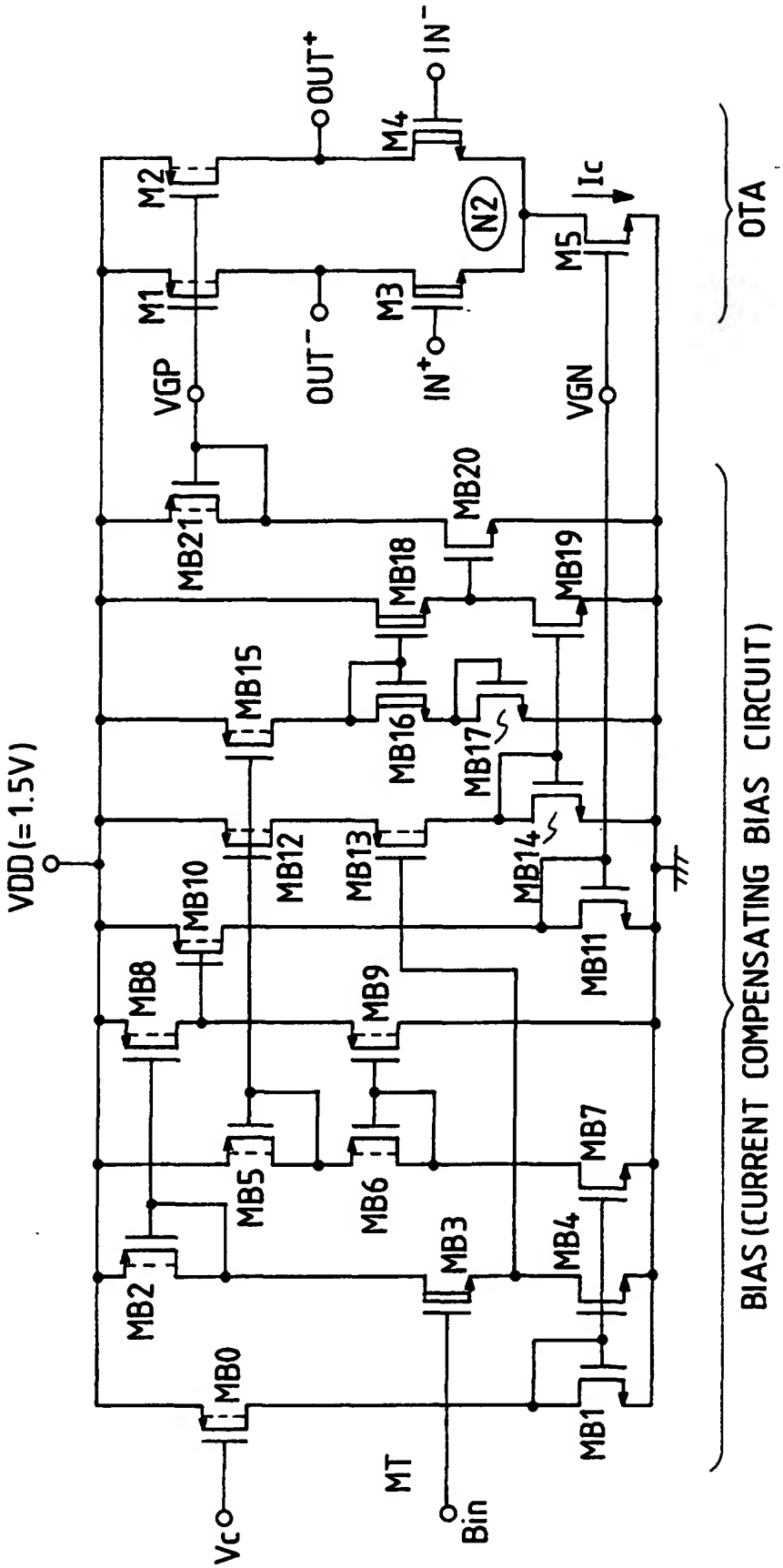
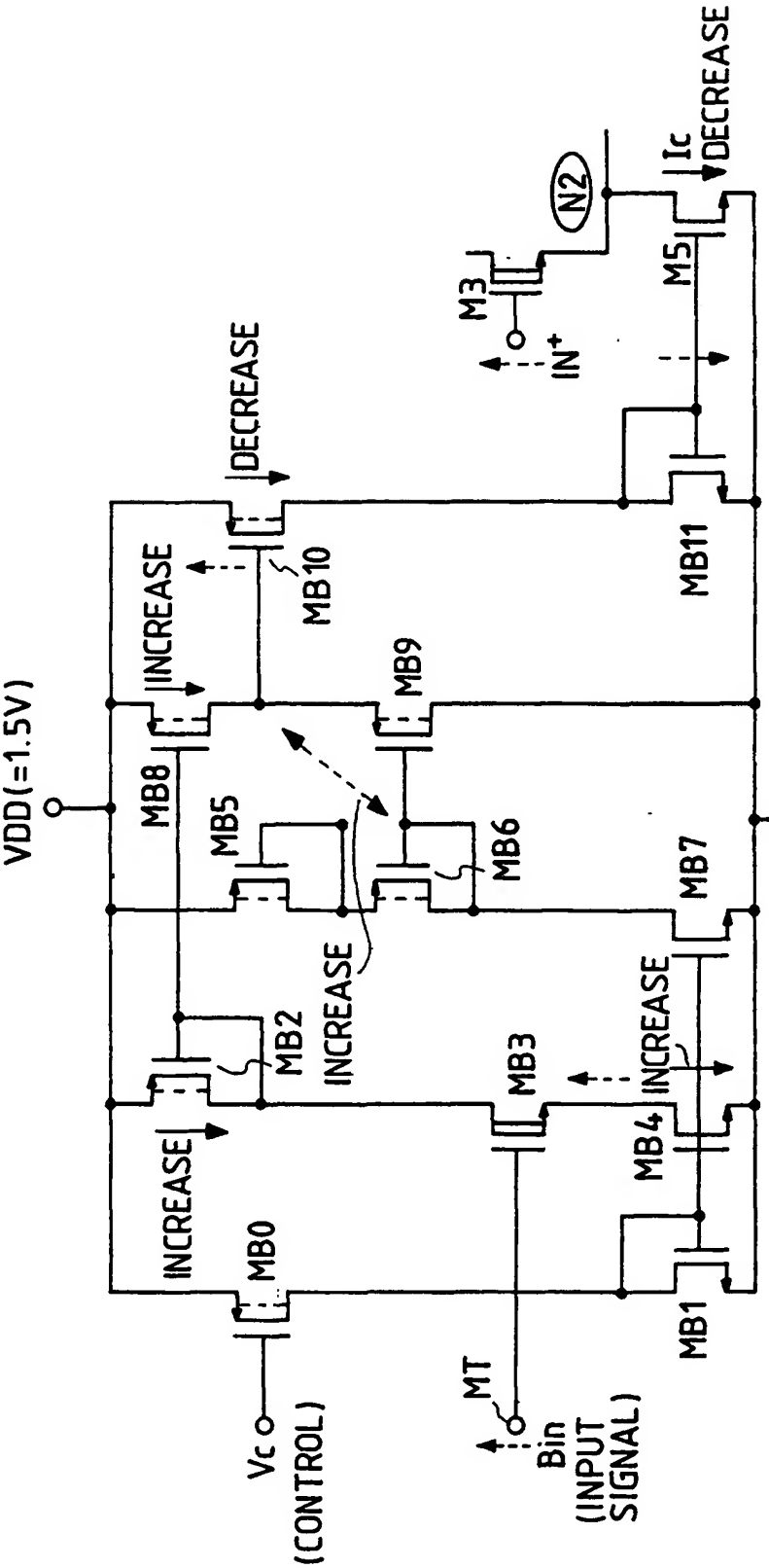

VDD(=1.5V)
OUT+
IN-
M4
M2
N2
Ic
M5
OTA
M1
M3
OUT-
IN+
VGP
VGN
MB21
MB20
MB18
MB19
MB15
MB16
MB17
MB12
MB13
MB14
MB10
MB11
MB8
MB9
MB5
MB6
MB7
MB3
MB4
MB2
MB0
MB1
MT
Vc
Bin
BIAS(CURRENT COMPENSATING BIAS CIRCUIT)

FIG. 6



CURRENT COMPENSATING BIAS CIRCUIT

FIG. 7

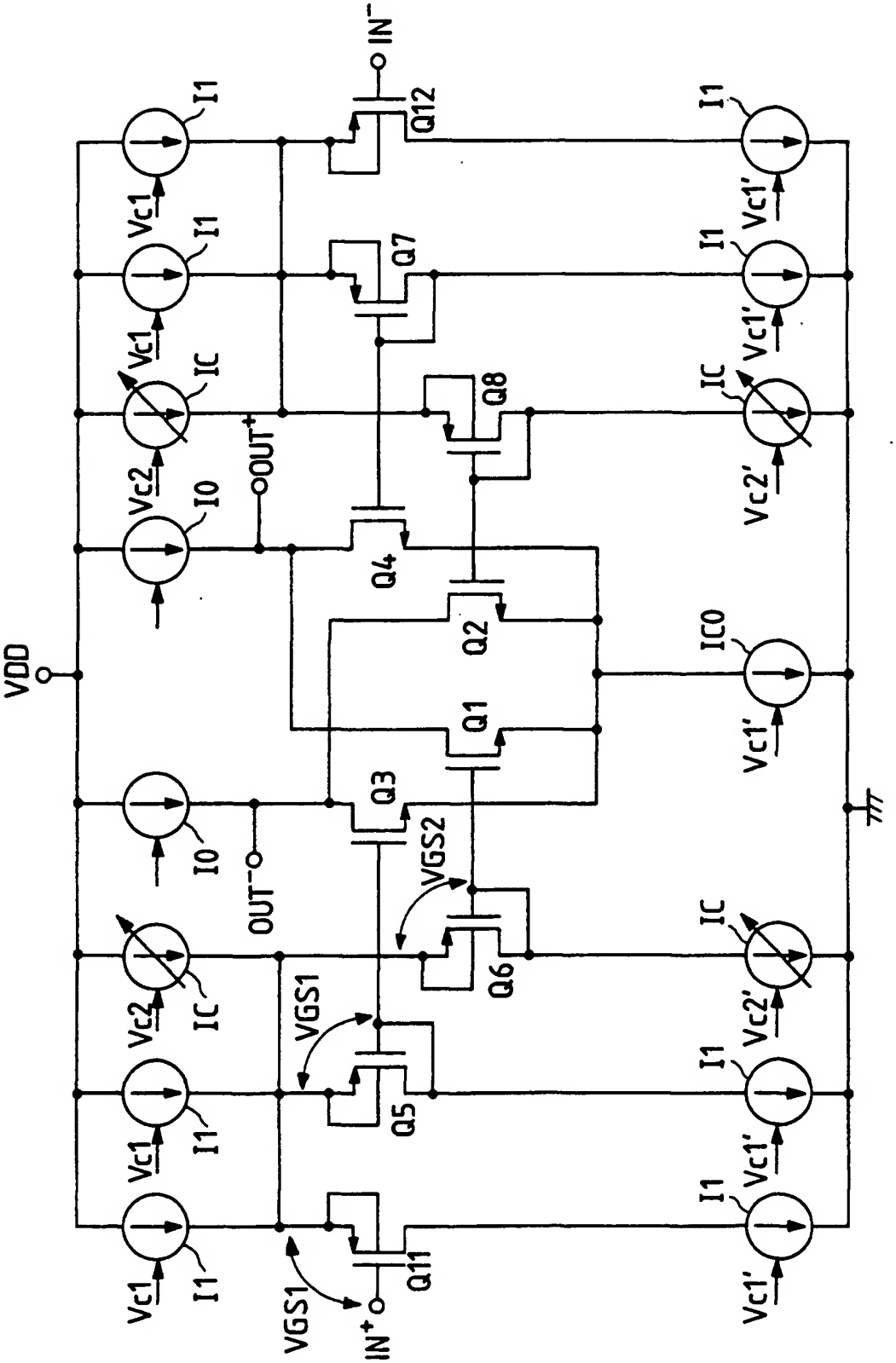
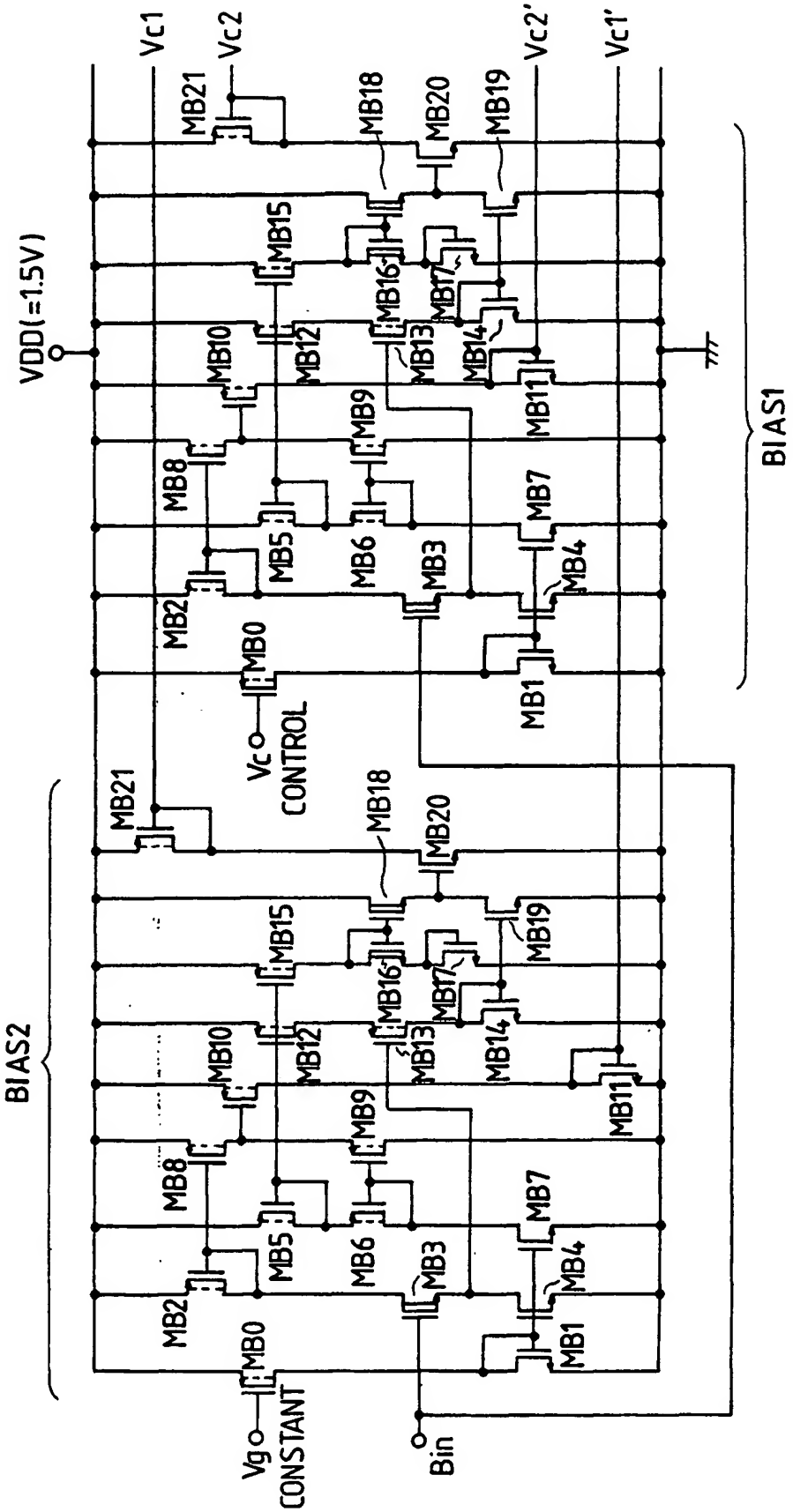

VDD
IN⁻
IN⁺
OUT⁺
OUT⁻
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q11
Q12
VGS1
VGS2
I0
I1
IC
IC0
Vc1
Vc2
Vc1'
Vc2'

FIG. 8


Vc1
Vc2
Vc2'
Vc1'
VDD(=1.5V)
BIAS1
BIAS2
Vc
CONTROL
Vg
CONSTANT
Bin
MB0
MB1
MB2
MB3
MB4
MB5
MB6
MB7
MB8
MB9
MB10
MB11
MB12
MB13
MB14
MB15
MB16
MB17
MB18
MB19
MB20
MB21

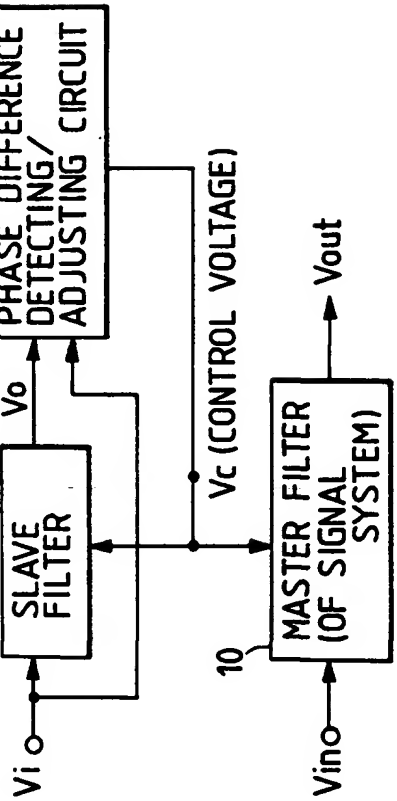

30
PHASE DIFFERENCE DETECTING/ ADJUSTING CIRCUIT
Vo
20
SLAVE FILTER
Vc (CONTROL VOLTAGE)
Vout
10
MASTER FILTER (OF SIGNAL SYSTEM)
Vi
Vino

FIG. 9

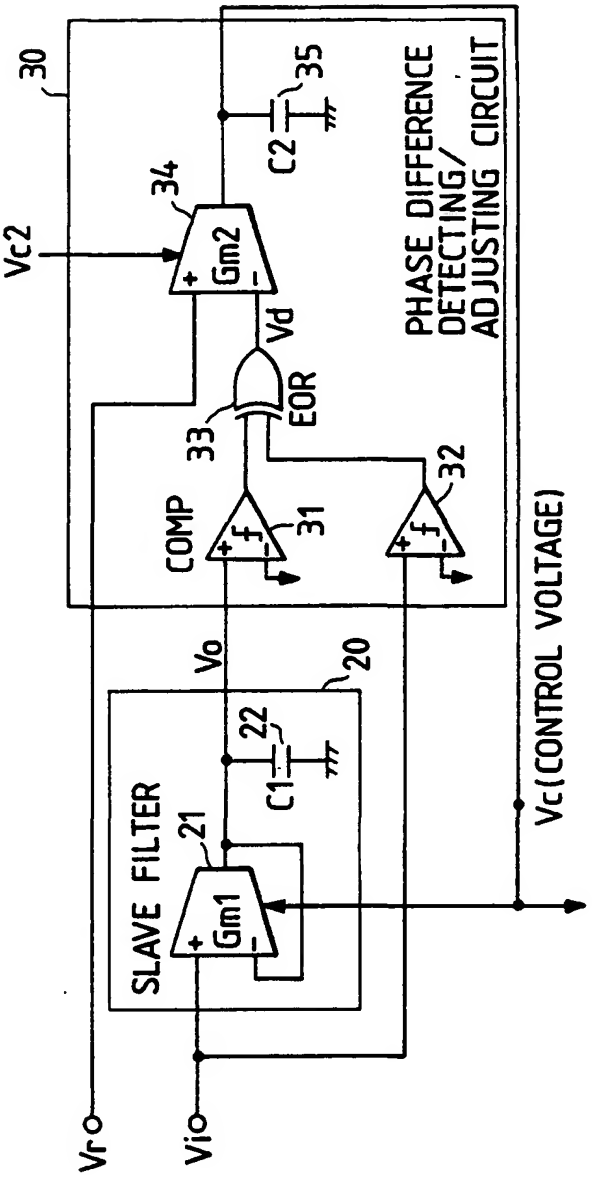

30
35
C2
34
Vc2
Gm2
Vd
PHASE DIFFERENCE DETECTING/ ADJUSTING CIRCUIT
33
EOR
COMP
31
32
Vo
20
22
C1
21
SLAVE FILTER
Gm1
Vc(CONTROL VOLTAGE)
Vr
Vio

FIG. 10

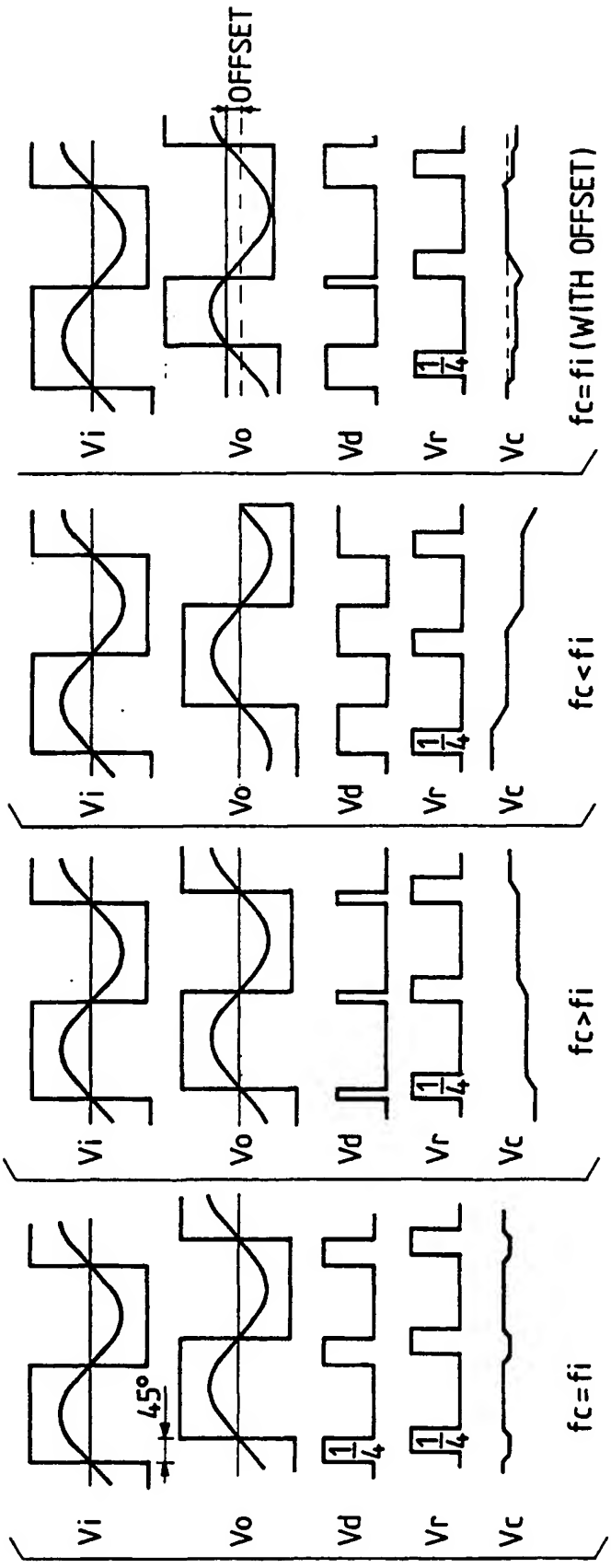


FIG. 11(a)
FIG. 11(b)
FIG. 11(c)
FIG. 11(d)
Vi
Vo
Vd
Vr
Vc
45°
OFFSET
1/4
fc=fi
fc>fi
fc<fi
fc=fi (WITH OFFSET)

FIG. 12

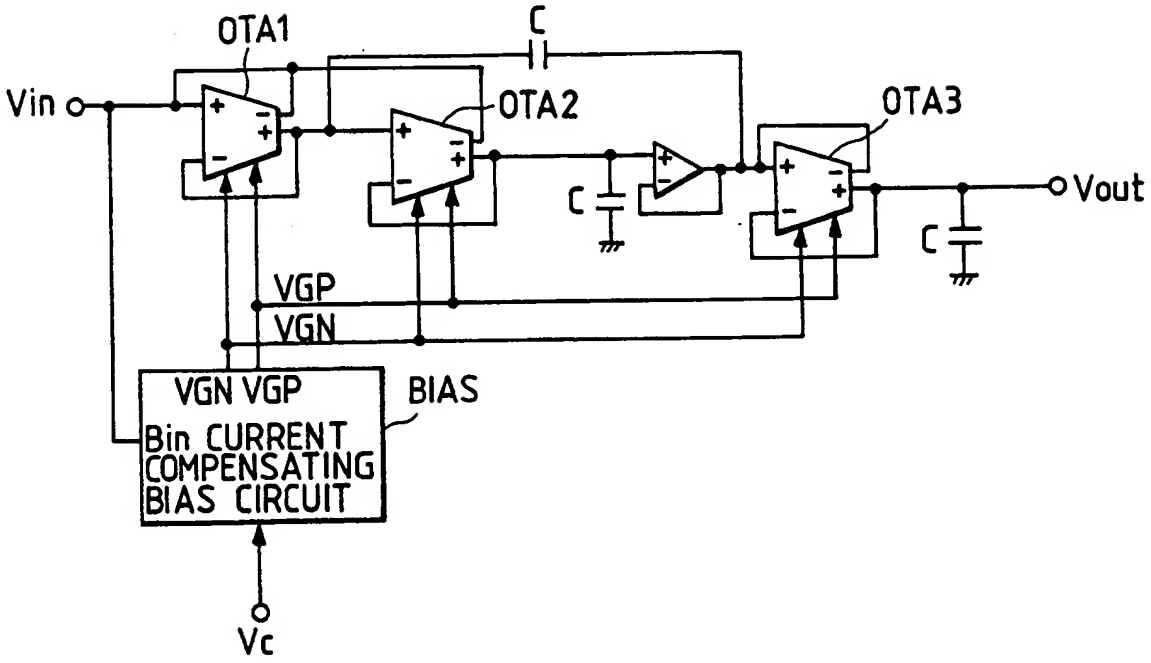

OTA1
C
Vin
OTA2
OTA3
Vout
C
C
VGP
VGN
VGN VGP
BIAS
Bin CURRENT
COMPENSATING
BIAS CIRCUIT
Vc

FIG. 13

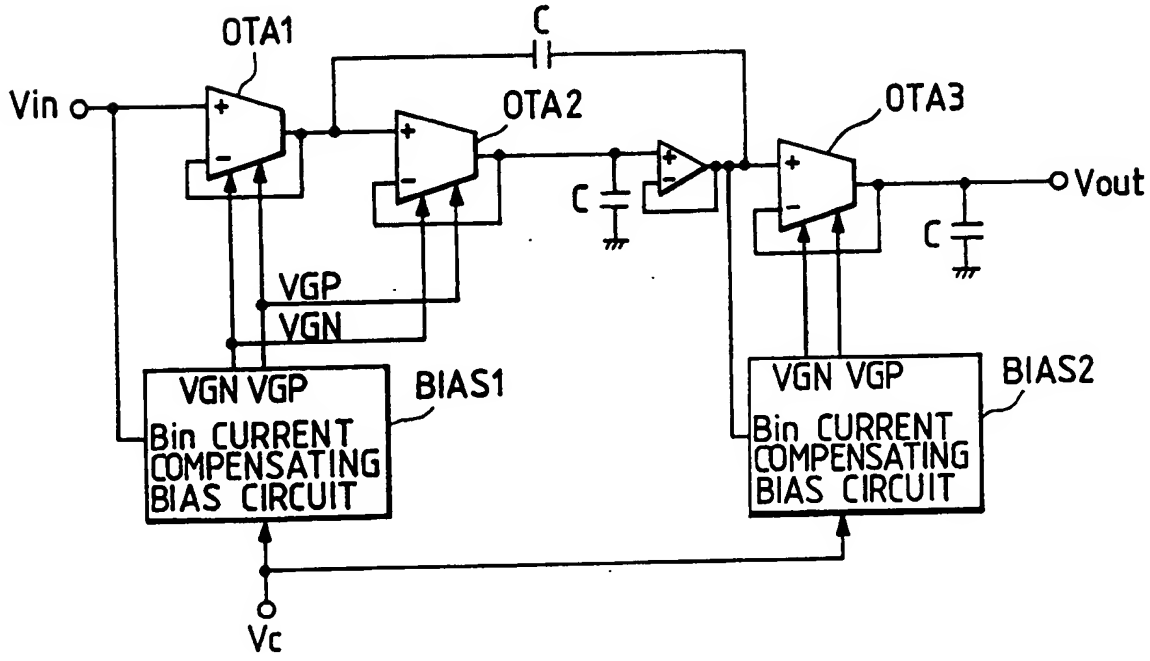

OTA1
C
Vin
OTA2
OTA3
Vout
C
C
VGP
VGN
VGN VGP
BIAS1
Bin CURRENT
COMPENSATING
BIAS CIRCUIT
VGN VGP
BIAS2
Bin CURRENT
COMPENSATING
BIAS CIRCUIT
Vc

FIG. 14

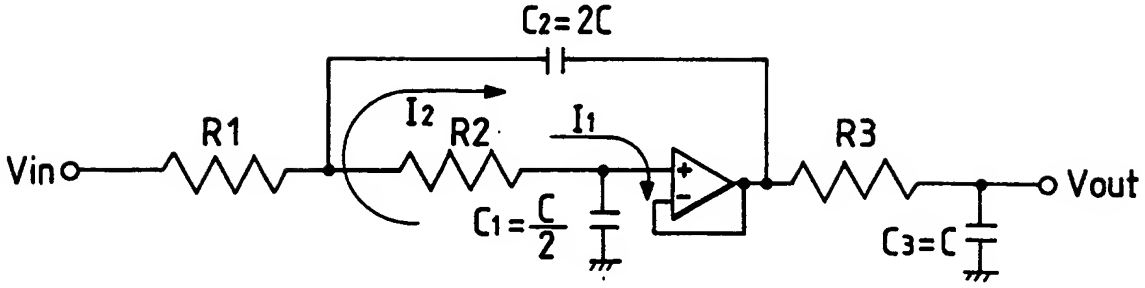

C2=2C
I2
I1
R1
R2
R3
Vin
Vout
C1=C/2
C3=C

FIG. 15

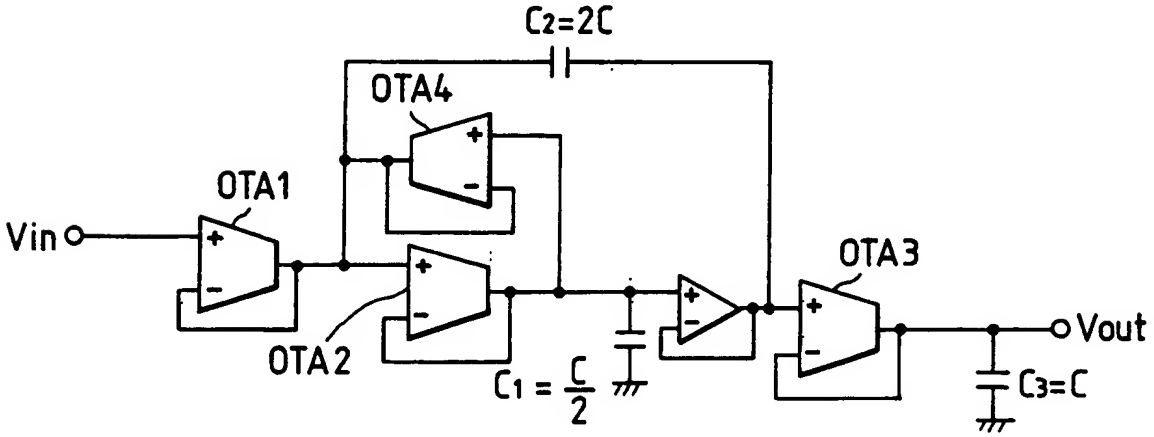

C2=2C
OTA4
OTA1
Vin
OTA3
Vout
OTA2
C1 = C/2
C3=C

FIG. 16

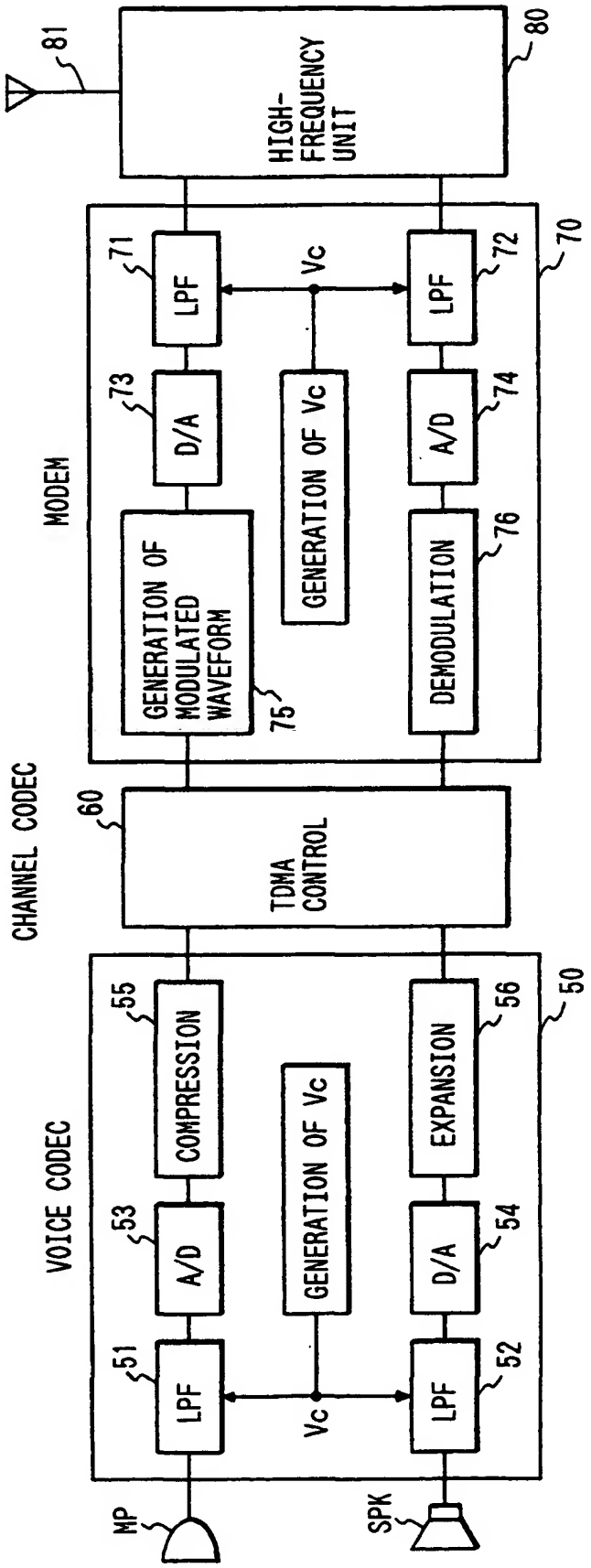

81
HIGH-FREQUENCY UNIT
80
MODEM
70
71
LPF
Vc
72
LPF
73
D/A
GENERATION OF Vc
74
A/D
GENERATION OF MODULATED WAVEFORM
75
DEMODULATION
76
CHANNEL CODEC
60
TDMA CONTROL
VOICE CODEC
50
55
COMPRESSION
56
EXPANSION
53
A/D
GENERATION OF Vc
54
D/A
51
LPF
Vc
52
LPF
MP
SPK

FIG. 17

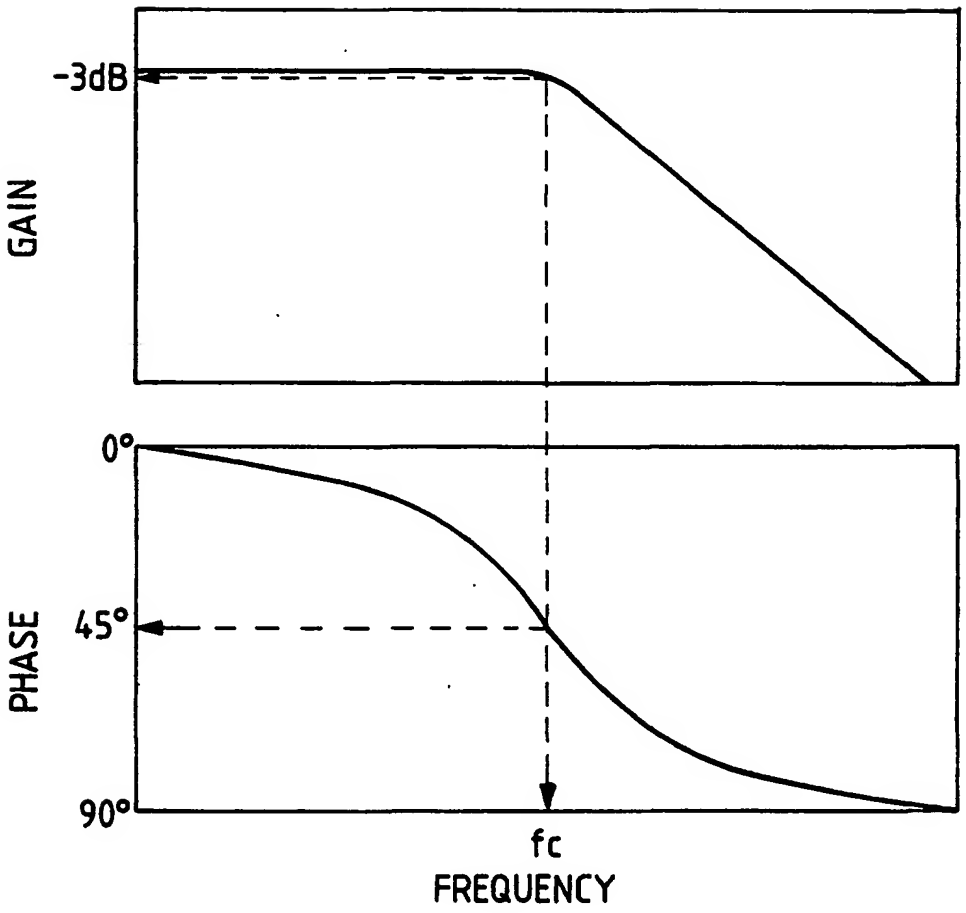


FIG. 18

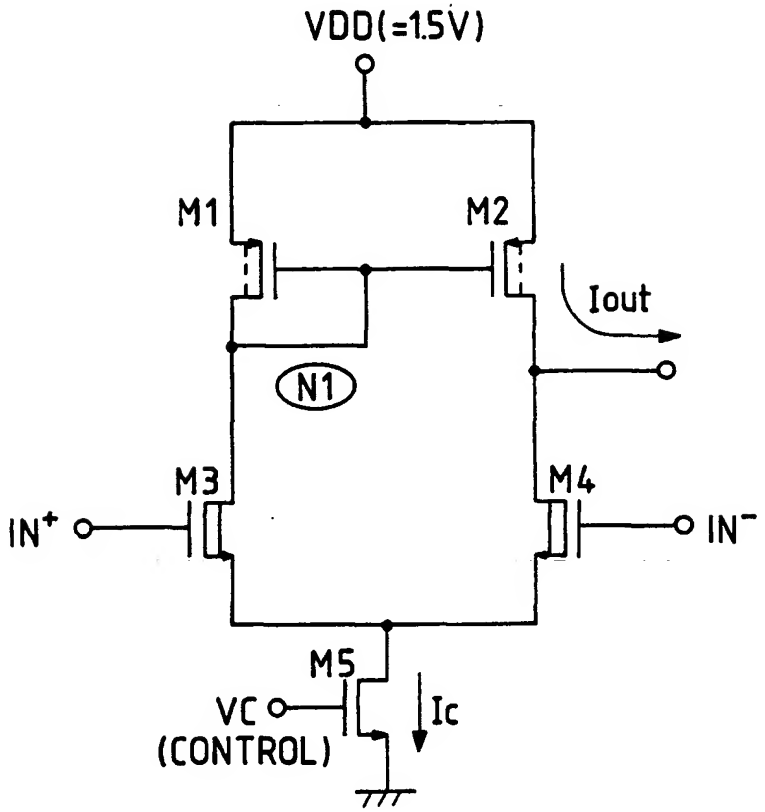


FIG. 19